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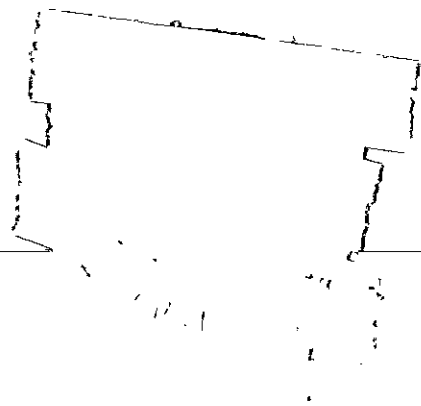
ULTRAMICROWAVE COMMUNICATIONS SYSTEM PHASE III

FINAL REPORT



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ULTRAMICROWAVE COMMUNICATIONS SYSTEM PHASE III

23 OCTOBER 1981

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FINAL REPORT

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I EXECUTIVE SUMMARY

Many space-to-space communication links will be required in the future to make full use of space operations. These links will require large data rates while minimizing interference with each other, with earth communications, and with earth-to-satellite links.

The 100-200 GHz band appears to be particularly favorable for meeting these requirements because this frequency range is used very little and because bandwidths (and thus data rates) can conceptually be very large. Private spectrum allocations can be used to obtain frequency isolation between carriers, as demonstrated by the charts shown in Figure 1. Small antennas can provide narrow beamwidths for isolation as well as producing large gain. Several large absorption peaks (Figure 2) are available that provide isolation from earth communications and up-and-down links. Compactness of the system and jamming resistance further enhance the attractiveness of using the 100-200 GHz band.

The Ultramicrowave Communications System (UCS) program was performed to investigate the feasibility of a solid state system that could meet the projected space-to-space requirements, while using the advantages of the 100-200 GHz band. The program successfully demonstrated a laboratory model of a high frequency communications system operating between 100-200 GHz. In the process, vendor claims for performance specifications of discrete components were evaluated, and a window was provided into present and future system design and integration problems.

WINDOW AND ABSORPTION BAND LIMITS

WINDOW	ABSORPTION BAND	LIMITS (GHZ)
W2		100-105
	A2	105-134
W3		134-170
	A3	170-190

SERVICE ALLOCATIONS

SERVICE	W2	A2	W3	A3	TOTAL
SATELLITE	14	2	7	4	27
SCIENTIFIC	5	5	5	5	20
TERRESTRIAL	24	5	14	8	51

FIGURE 1: SUMMARY OF FCC ALLOCATIONS FROM 100-200 GHZ

1.1 Approach

The program was divided into three phases. In Phase I a survey of current research and development activities at millimeter wave frequencies was performed, and a search for vendors of RF hardware was initiated to determine component availability and implement first order system design.

In Phase II a preliminary design of the RF subsystem was completed, and a packaging study was performed to determine a minimum size of the system. Also, the required RF hardware for the subsystem design was procured.

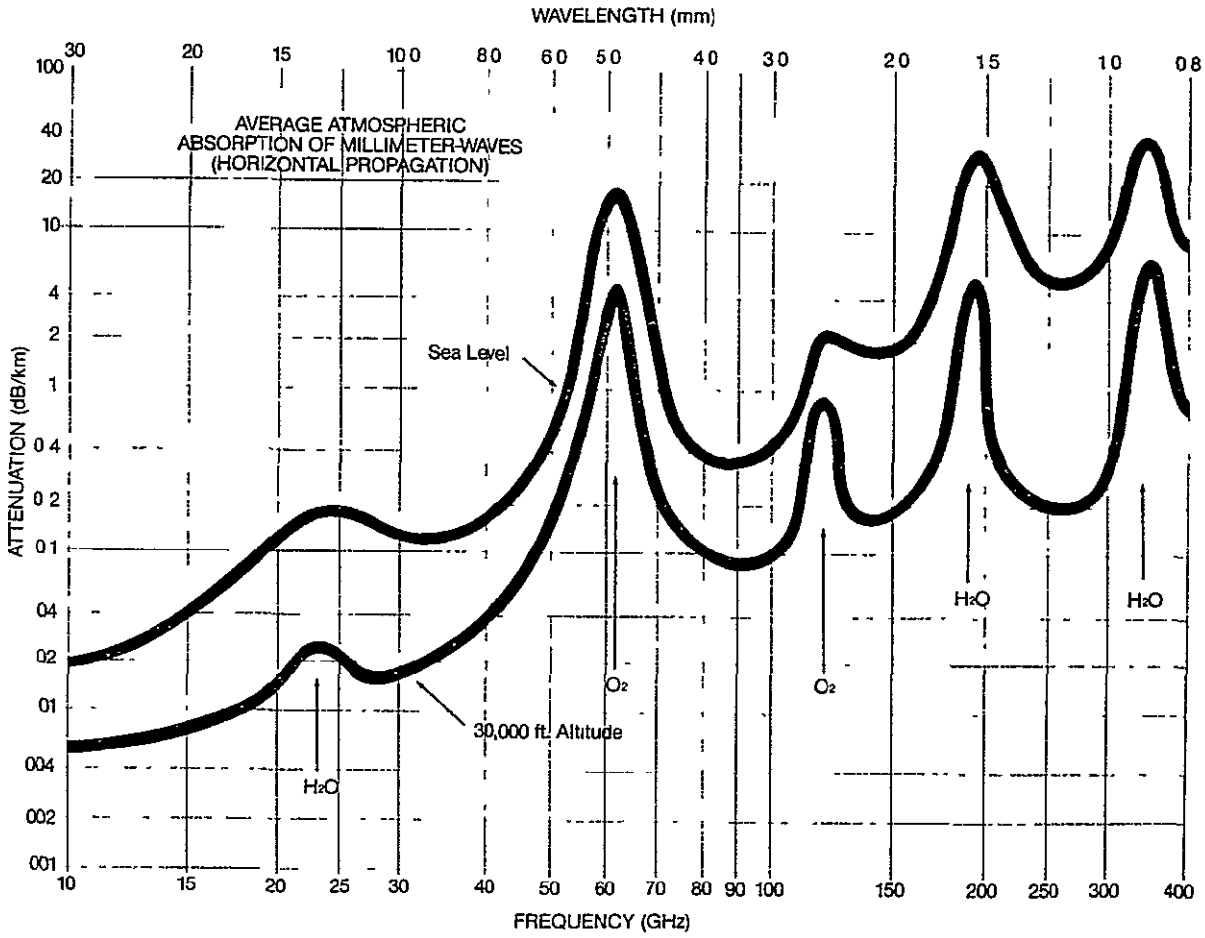


FIGURE 2: ATMOSPHERIC ATTENUATION OF MILLIMETER WAVES

In Phase III the remainder of the system design and hardware procurement was completed, the final demonstration unit was assembled, and system tests were performed. Finally a system demonstration was given at NASA/JSC.

1.2 Results

We successfully designed and built a low cost transmitter/receiver demonstration unit using off-the-shelf millimeter wave components. The system uses bi-phase modulation to transmit a 130 Mb/s bit serial stream at a carrier frequency of 105 GHz over a range of approximately 100 meters. Figure 3 shows a

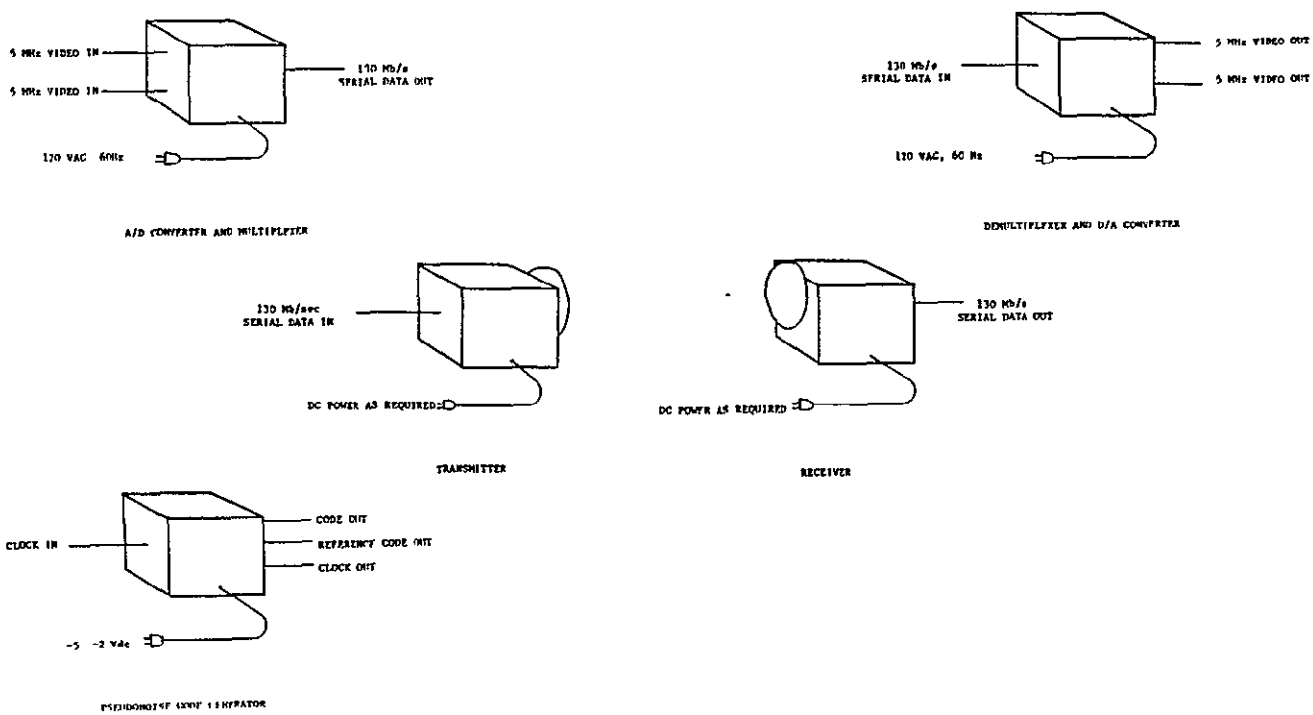


FIGURE 3: ULTRAMICROWAVE COMMUNICATIONS SYSTEM AND SUPPORT EQUIPMENT

block diagram of the system and its support equipment.

Several key development problems were solved to construct the system. For example, the carrier frequency of 105 GHz was chosen because the required RF hardware was only available at the lower end (to 110 GHz) of the 100-200 GHz spectrum. (Table 1 shows a chart of component availability for various frequency ranges.)

Although off-the-shelf components were available at 105 GHz, conformance to vendor specs was very poor with regards to noise figure, lifetime, etc. The RF system design had to be compensated for matching and isolation problems between devices, as well as instability and poor noise figure of discrete components. Further, delivery times ranged up to one year.

	HUGHES	VARIAN	THOMSON – CSF	PLESSEY	ENGLISH ELEC VALVE	SIEMENS	BAYTRON	TORNGREN/SPINCRAFT	75 - 110 GHZ	97 140 GHZ	110- 170 GHZ	140 220 GHZ
RF SOURCE (CW)	X	X*		X*	X*	X*			X	X*	X*	X*
MODULATORS	X	X					X		X			
RF AMPLIFIERS	X								X			
CIRCULATORS	X		X						X			
HORNS			X				X		X	X	X	X
MIXERS (FUNDAMENTAL)	X						X		X	X		
MIXERS (HARMONIC)	X						X		X	X		
LOCAL OSCILLATORS (RF)	X	X*		X*		X*			X	X*	X*	X*
LOCAL OSCILLATORS (IF)	X	X	X	X		X						
IF AMPLIFIERS	X	X	X									
WAVEGUIDE COMPONENTS	X		X				X		X	X	X	X
ANTENNAE								X	X	X	X	X

*SOLID-STATE NOT AVAILABLE

TABLE 1: RF SUBSYSTEM COMPONENT AVAILABILITY

The development of a driving circuit for the bi-phase modulator was a key development in the design of the system, as none was readily available for our purposes. The circuit was designed to provide the proper levels to the diode of the modulator for the two phase states. It is also capable of handling the 130 Mb/s data rate.

Support equipment which had to be developed for the UCS includes: the A/D Converter Multiplexer Subsystem, Demultiplexer D/A Converter Subsystem, and Pseudo Random (PN) code generator. The A/D Converter Multiplexer Subsystem (ADCMS) interfaces two 5 MHz analog video signals with the digital input to the transmitter. The Demultiplexer D/A Converter Subsystem (DDACS) interfaces the digital receiver output with two analog channels. It converts the receiver output back to the two original 5 MHz video signals. The PN code generator produces a 127 - bit digital code synchronous with an external clock. It was used for checkout and testing of various digital circuitry in the system modules. (Appendix H contains a schematic of the PN code generator shown in drawing 5).

1.3 Conclusions

The UCS program demonstrated the performance possible in a communications system built to be operated above 100 GHz. While large performance improvements could be realized with available components (at a higher cost), performance deficiencies exist in several areas.

The apparent limitations to higher data rates are the clocking frequencies of signal processing components, and the switching speed of the modulator driver between the two phase states.

Operation is possible with available off-the-shelf RF components, but performance predictions must be tempered by poor component tolerances. The low cost system demonstrated a 130 Mb/s channel over 100 meters. Immediately available components should permit ranges up to 45 km.

During the final phase of the program a substantial amount of time was required for the design and construction of the high data rate signal processing subsystems (ADCMS, DDACS). In a fully operational system, handling and processing the data prior to modulation of the carrier and after detection in the receiver will be a major task requiring careful design of high speed logic circuits.

Although a demonstration unit has been assembled, further work in the areas of millimeter wave component development, systems itegration, and signal processing system development needs to be done before ultramicrowave systems will be able to meet future space communications requirements.

II UCS SYSTEM AND DEMONSTRATION

The UCS demonstration consisted of using the transmitter and receiver to transmit spread spectrum data in a laboratory environment. Also during the demonstration, system tests and performance analysis were done. A description of each subsystem is given in this section, along with details of how the demonstration was implemented. Further, results of the tests and analysis are given.

2.1 System Description

The Ultramicrowave Communications System consists of the transmitter module and receiver module. A description of each subsystem is given below.

2.1.1 Transmitter

The transmitter subsystem consists of: the RF front end, high gain antenna modulator driver, and required power supplies. A block diagram of the system is shown in Figure 4. The input is an ECL (emitter coupled logic) level serial signal that is transformed to the proper levels by the modulator driver. The transformed data drives the modulator to shift the carrier phase between 0° and 180° (bi-phase modulation). The carrier is a 104.725 GHz millimeter wave signal generated by a free running oscillator. The modulated signal is then transmitted via the parabolic antenna. Figure 5 shows a block diagram of the active RF components. Photographs of the transmitter are shown in Figure 6. (For more detail see appendix B.)

2.1.2 Receiver

The receiver subsystem consists of: a high gain antenna, RF front end, IF amplifier strip, demodulator and required power supplies. A block diagram of the

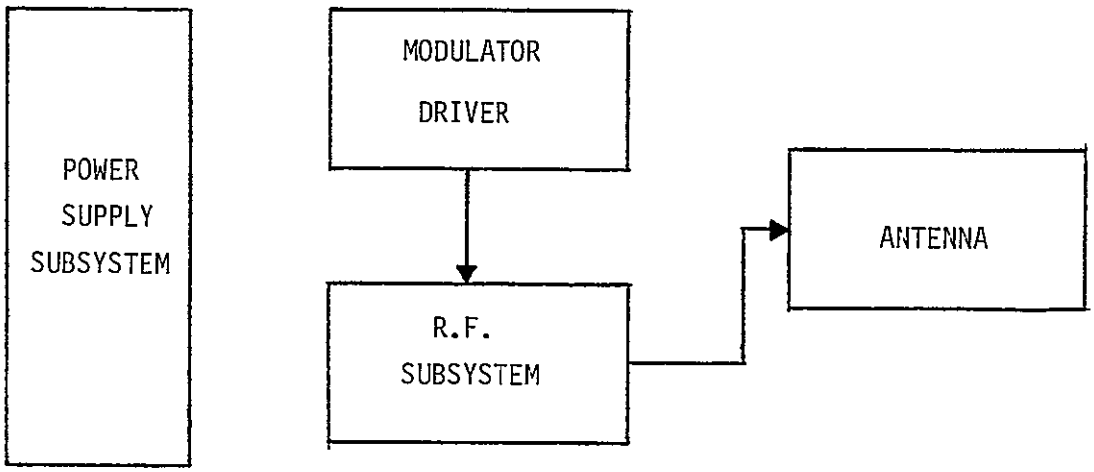


FIGURE 4: BLOCK DIAGRAM OF TRANSMITTER

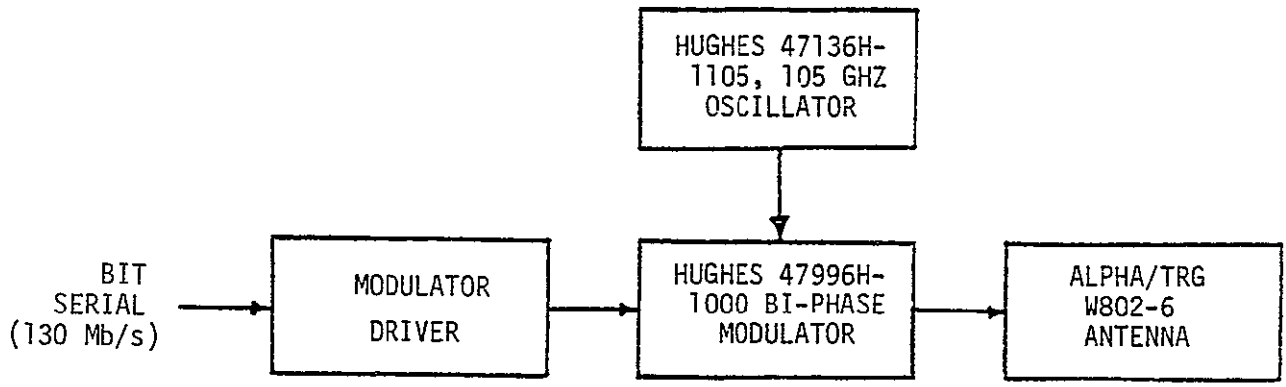


FIGURE 5: TRANSMITTER ACTIVE COMPONENTS

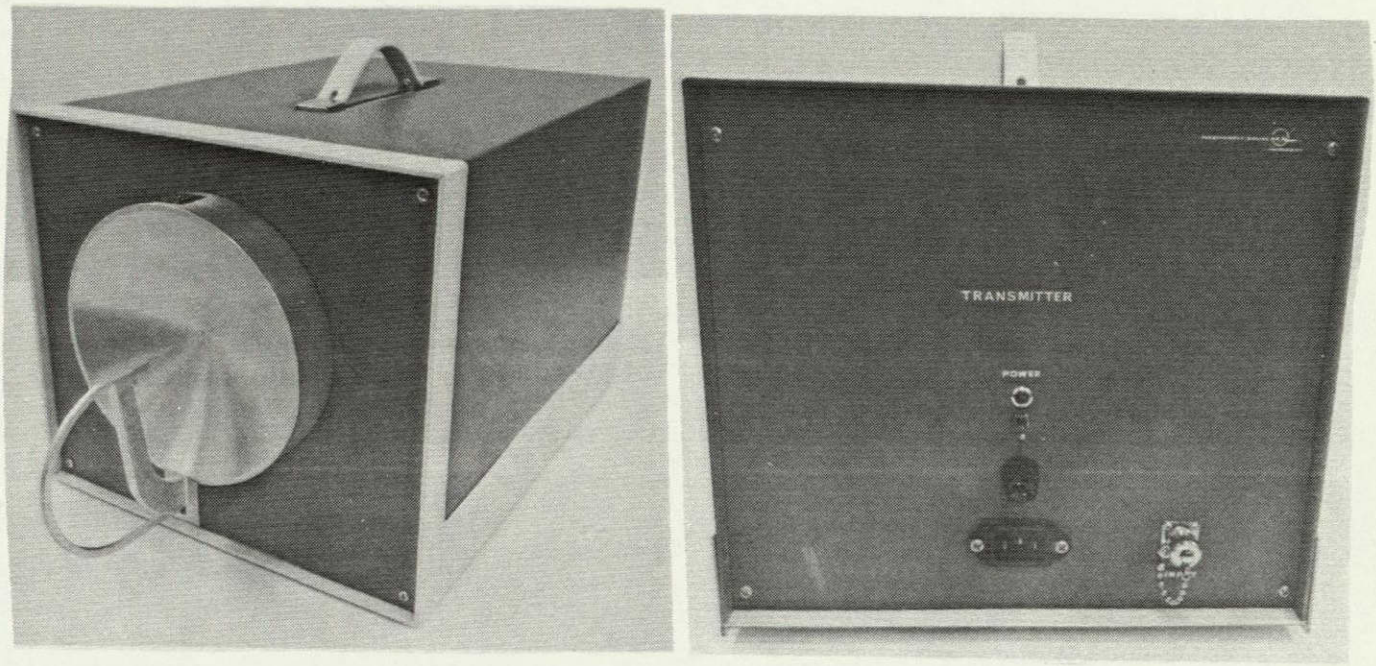


FIGURE 6: ULTRAMICROWAVE COMMUNICATIONS TRANSMITTER

subsystem is shown in Figure 7. This module receives the bi-phase modulated signal via the parabolic antenna. This signal is down converted to an IF frequency of 273 MHz, by mixing it with an LO (local ocillator) signal in the harmonic mixer. The LO signal is a 14.93 GHz signal generated by a Gunn oscillator. The signal is amplified in the IF section for input to the demodulator. The bi-phase demodulator transforms the signal to a ECL digital stream. The output is a serial digital data signal of up to 130 Mb/S. Tuning of the receiver is facilitated by fine and course adjustment tuning knobs that control the LO frequency. A block diagram of the active RF components is shown in Figure 8. Photographs of the receiver are shown in Figure 9. (For more detail see appendix C.)

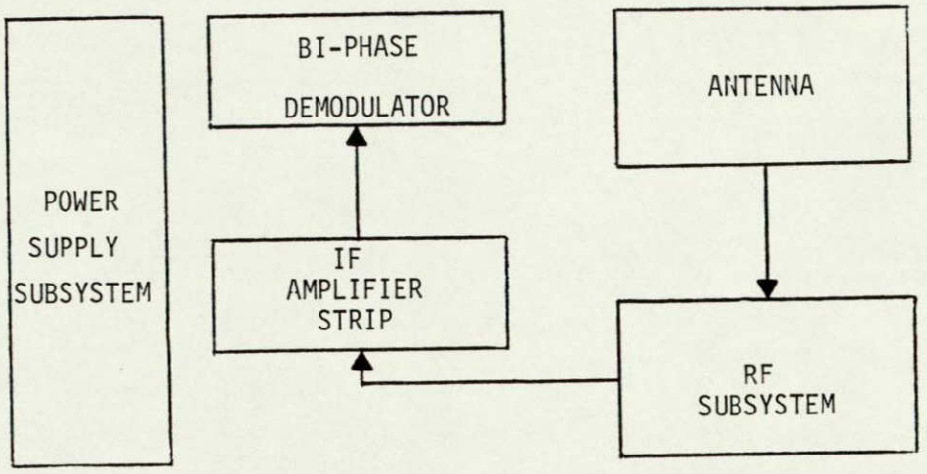


FIGURE 7: BLOCK DIAGRAM OF RECEIVER

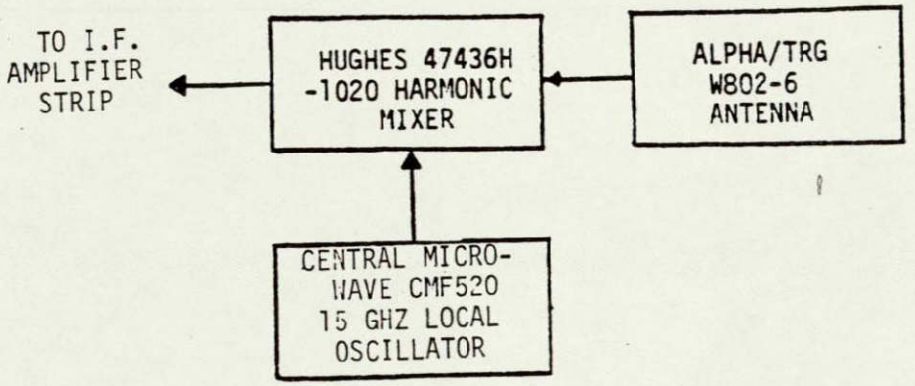


FIGURE 8: RECEIVER ACTIVE RF COMPONENTS

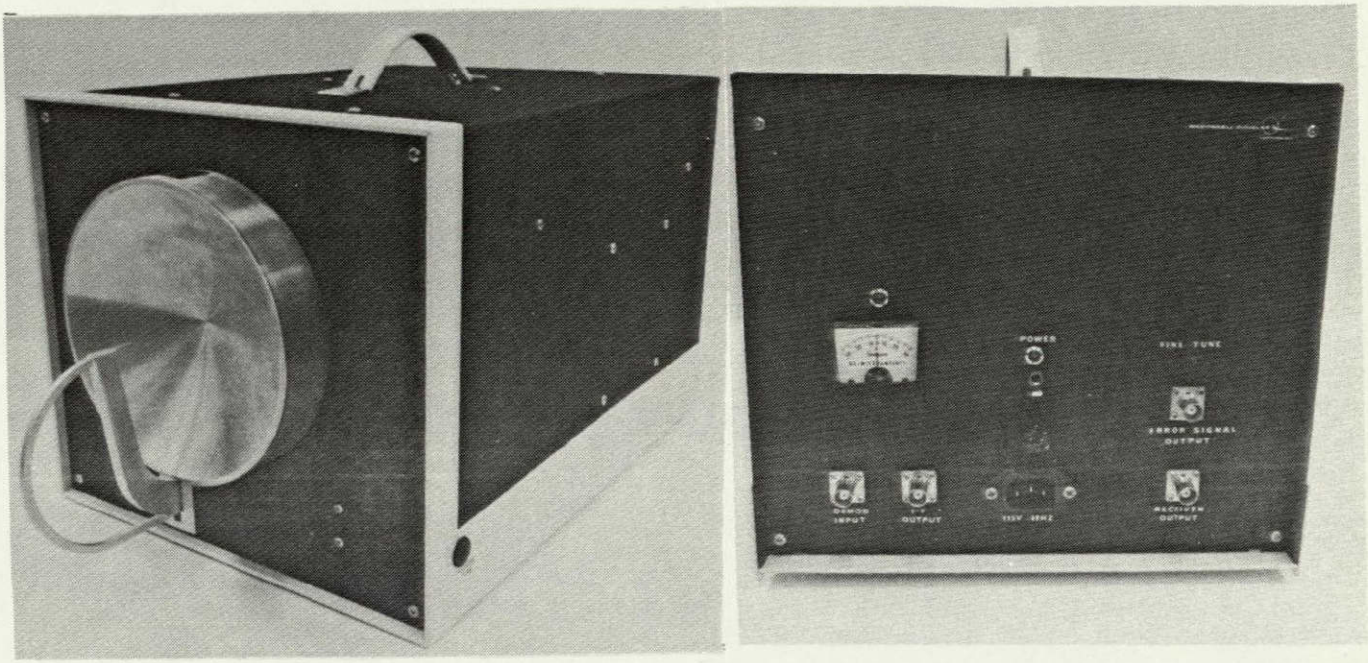


FIGURE 9: ULTRAMICROWAVE COMMUNICATIONS RECEIVER

2.2 UCS Demonstration

This section gives a general description of the demonstration, followed by the results of the performance analysis and tests.

2.2.1 Description of Demonstration Set Up

The demonstration of the UCS consisted of transmitting and monitoring two 5 MHz color video signals in a laboratory environment.

The test signals were generated by two color cameras, viewing the laboratory, interfaced to the transmitter via the ADCMS. The ADCMS contains two A/D converters, a multiplexer, a synchronization circuit, and a differential encoder. The A/D converters sample each test signal at a 10 megasample/second

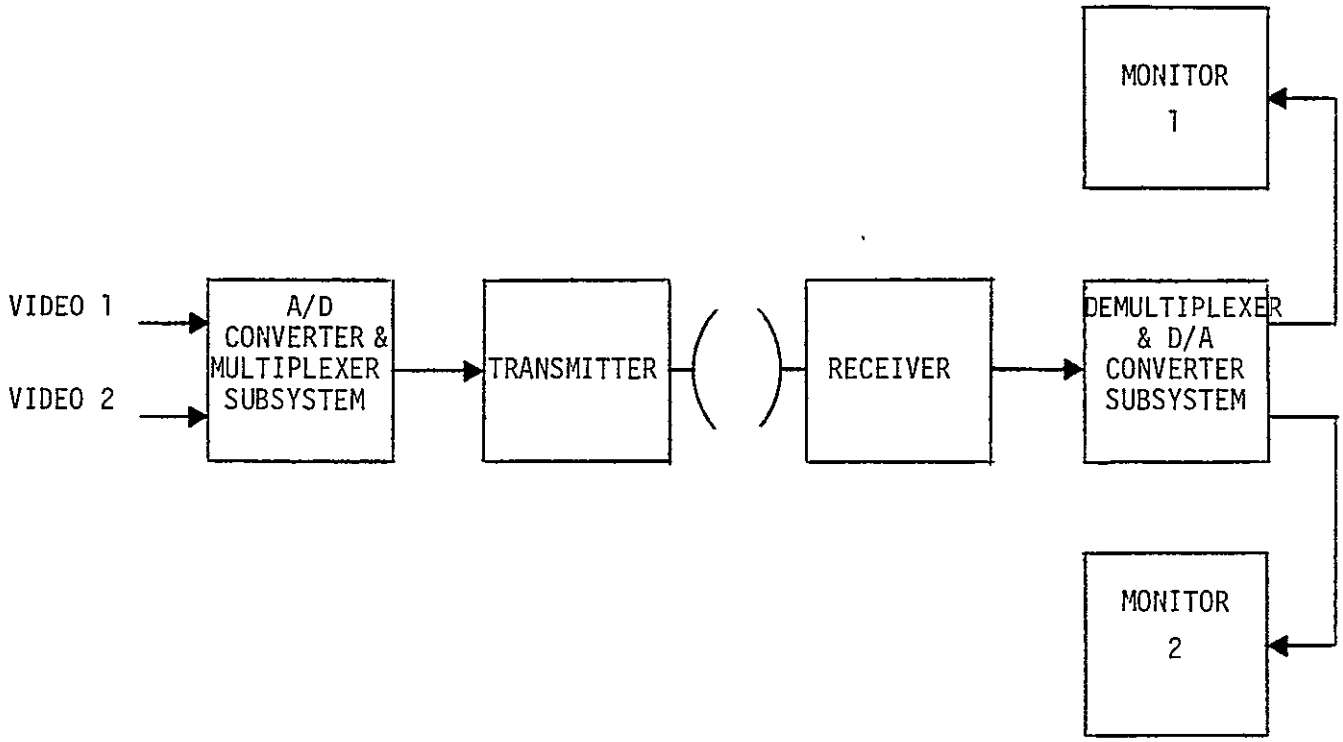


FIGURE 10: UCS DEMONSTRATION SETUP

rate, and quantizes each channel to six bits. The output is a differentially encoded 130 Mb/s ECL serial stream. (For more detail of the ADCMS see Appendix D.)

The received signals are interfaced to two color monitors by the DDACS. This module contains a clock recovery circuit, differential decoder, demultiplexer with synchronizing circuits, and two video D/A converters. The input is the recovered 130 Mb/second ECL serial data stream recovered from the demodulator. This signal is split into the two six bit digital channels by the demultiplexer-synchronization circuitry, using the clock signal recovered from the data stream. The D/A converters sample each channel to produce the analog signals. The output is the two 5 MHz bandwidth video signals. (For more detail on the DDACS see Appendix E.) Figure 10 shows the demonstration setup.

2.2.2 Demonstration

The purpose of the demonstration was to evaluate system performance. This included measurements of antenna performance, range prediction, and overall signal quality. Signal quality was evaluated by spectrum analysis of the transmitted signal as well as by monitoring the transmitted video pictures, and making predictions of bit error rate and signal/noise.

Figure 11 shows plots of the pattern of the 6 inch parabolic antenna, in both the E and H planes. As can be seen the 3 dB beamwidth is 1.25° in the E plane and 1.40° in the H plane. The antenna gain is 42 dB which illustrates the advantage of small size and large gain available at the short wave length.

Range of the system was simulated by inserting a variable attenuator into the output of the transmitter. It was found that an attenuation 25 dB was obtained before the signals on the video monitors were no longer recognizable. This results in a theoretical maximum range of 103 meters.

A spectrum of the UCS modulated signal is shown in Figure 12 and a expanded view is shown in Figure 13. A perfectly bi-phase modulated signal should exhibit a zero-amplitude carrier, so these measurements indicate that proper modulation is not being obtained. An amplitude imbalance of .94 dB was measured between the two phase states of the modulator, which would contribute to the non-optimum modulation. Also a phase imbalance was likely present, however this was not measured directly.

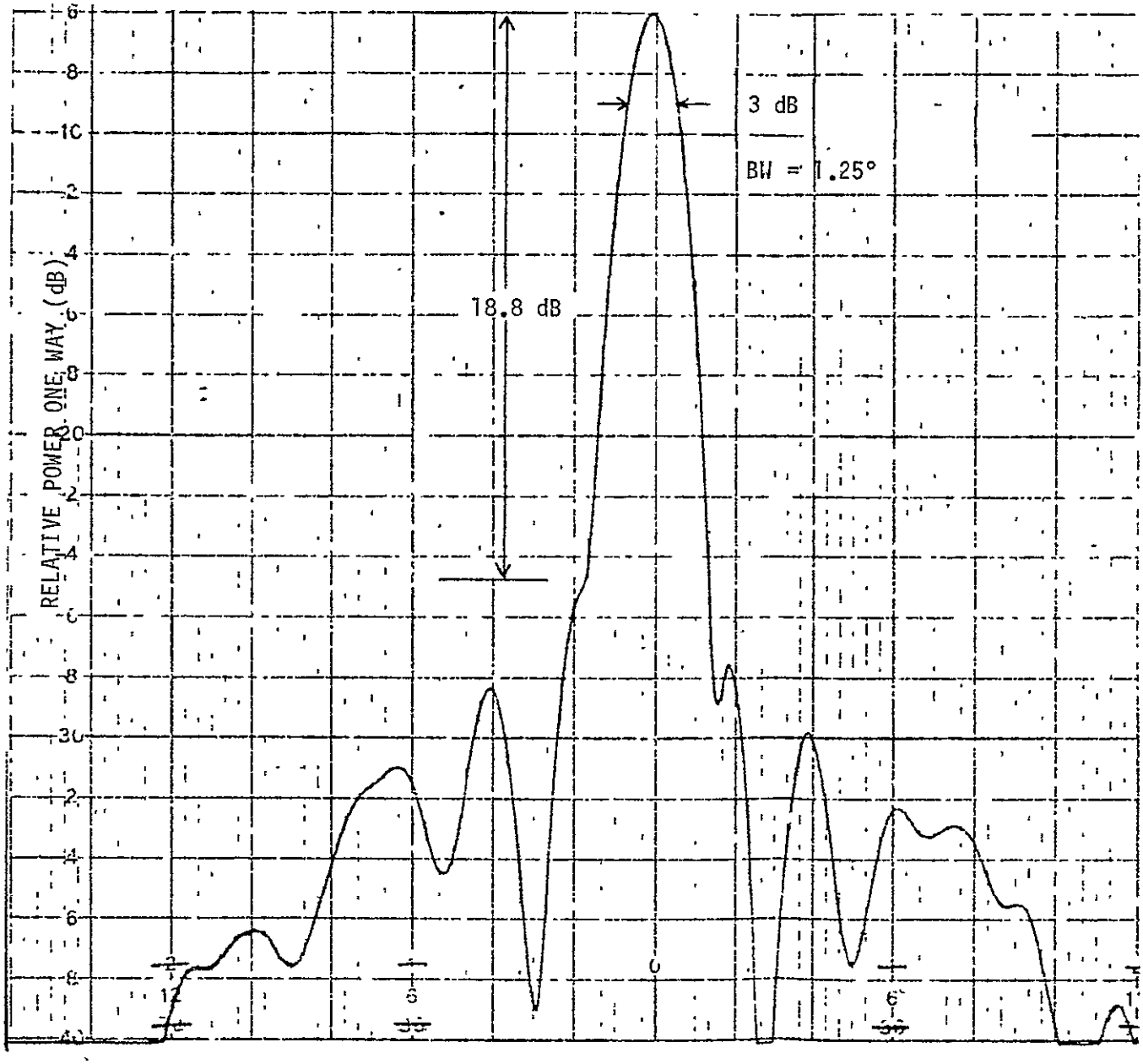
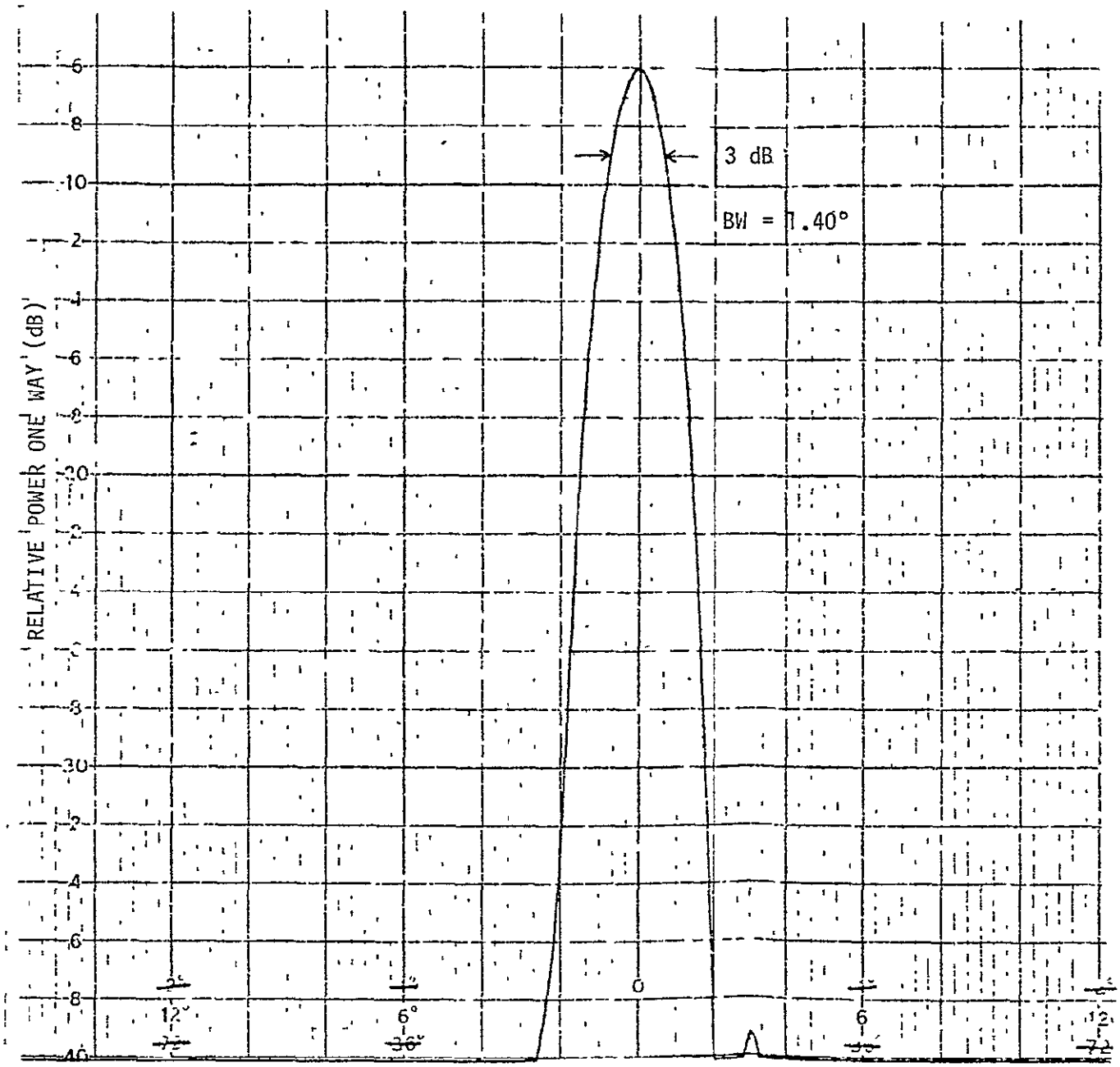


FIGURE 11A: E PLANE PATTERN OF 6 INCH PARABOLIC ANTENNA AT 104.725 GHZ



ANGLE

FIGURE 11B: H PLANE PATTERN OF 6 INCH PARABOLIC ANTENNA AT 104.725 GHZ

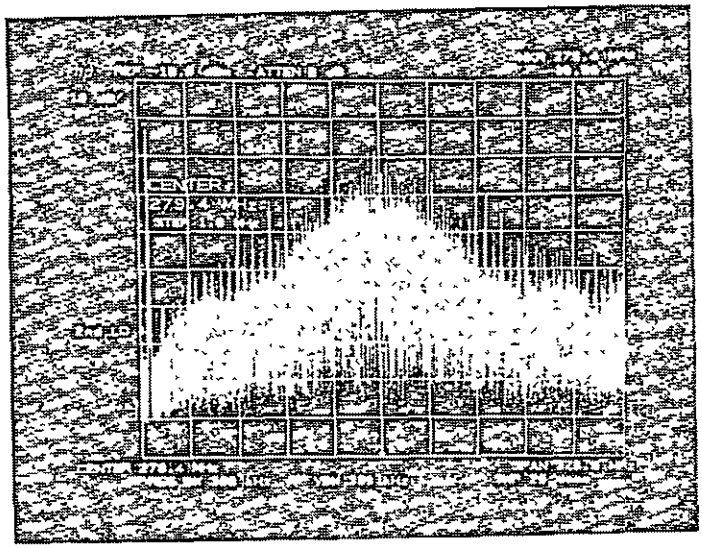


FIGURE 12: SPECTRUM OF TRANSMITTED UCS SIGNAL

HORIZONTAL SCALE: 10 dB/DIV
REFERENCE LEVEL: -10 dBM
VERTICAL SCALE: 37.6 MHZ/DIV
CENTER FREQUENCY: 279.4 MHZ

Although overall quality of the video pictures on the monitors was good, some bit errors were noticed. Also loss of synchronization errors were present which caused the receiver to lose lock with the transmitted data. Fine and coarse tuning of the receiver was periodically required in order to retain the video pictures. From the quality of the video pictures on the monitors we estimated the signal/noise of the video signal to be 20 to 30 dB.

The amount of bit and synchronization errors (noise) in the system could be attributed to two possible factors; amplitude and phase noise. Various separation distances between the transmitter and receiver, (from approximately 1 ft. to 50 ft.) did not significantly alter the amount of errors. Also attenuation of the signal during range simulation tests did not change the amount of errors (above the threshold of the minimum detectable signal). Therefore, although some

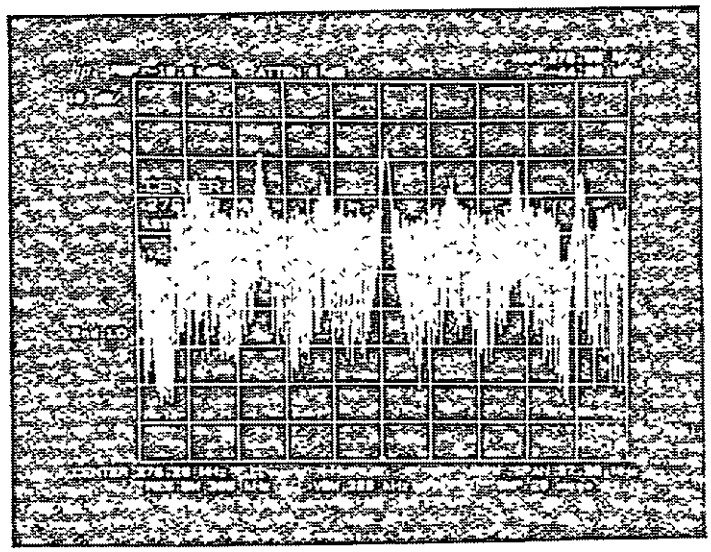


FIGURE 13: EXPANDED VIEW OF TRANSMITTED SPECTRUM

HORIZONTAL SCALE: 10 dB/DIV
REFERENCE LEVEL: -10 dBM
HORIZONTAL SCALE: 3.76 MHZ/DIV
CENTER FREQUENCY: 276.2 MHZ

amplitude noise was likely present, it was not the major contributing factor to errors.

The main source of noise was probably due to phase instabilities in the system. The Gunn oscillator used in the transmitter had a significant amount of frequency drift and thus contributed to phase noise. Measurements of this frequency drift were taken and are shown in Appendix B. Also the local oscillator had some frequency drift, measurements of which are shown in Appendix C.

Detuning of the oscillator occurred with changes in the modulator phase state. This of course would add considerably to the phase noise of the system. This problem was corrected, for the most part, by insertion of isolators between the oscillator and modulator (see Appendix B). With one isolator the frequency

change between the two phase states was 650 KHz. With two isolators, no noticable change could be detected in frequency. The required addition of these isolators to obtain acceptable operation indicates that the performance of the modulator is less than optimum. This is also supported by measurements taken with no isolation, which showed a 12.5 MHz change in frequency of the oscillator for changes in phase state of the modulator.

Random phase noise from other parts of the system also added to the overall noise in the video pictures. Howver this was not directly measurable due to equipment limitations.

III RECOMMENDATIONS

The UCS demonstration shows the level of performance available from a low cost approach to ultramicrowave communications. The current design was chosen to evaluate individual component performance and was limited by cost constraints. This section recommends immediate improvements which could be made on the system using currently available hardware and design concepts.

The noise figure of the receiver (and S/N ratio of the system) could be improved by replacing the harmonic mixer with a balanced mixer/IF preamplifier. The harmonic mixer has a conversion loss, at the 7th harmonic, of 23 dB, while the noise figure of a balanced mixer is 5.5 dB. Although the cost of the balanced mixer is considerably larger, the improvement in receiver noise figure is substantial. (The harmonic mixer was chosen mainly due to cost limitations.)

Several options are available which would provide a more stable millimeter wave source. Bias tunable Gunn oscillators are available which can be phase locked to a stable crystal source. This would decrease phase noise in the system and provide easier demodulation. These oscillators are available with power outputs to 20 mW. Clearly this would increase the range of the system and improve S/N. However, these oscillators are only available to 95 GHz. Therefore a lower carrier frequency would have to be chosen for use of this approach.

Other approaches available to improve the performance of the system include injection locking and frequency multiplying techniques. Injection locked IMPATT oscillators are available to 100 GHz with a power output of 50 mW. The IMPATT oscillator can be used as a power amplifier by injection locking it to a phase stabilized Gunn source. The maximum locking bandwidth of the IMPATT is .5%.

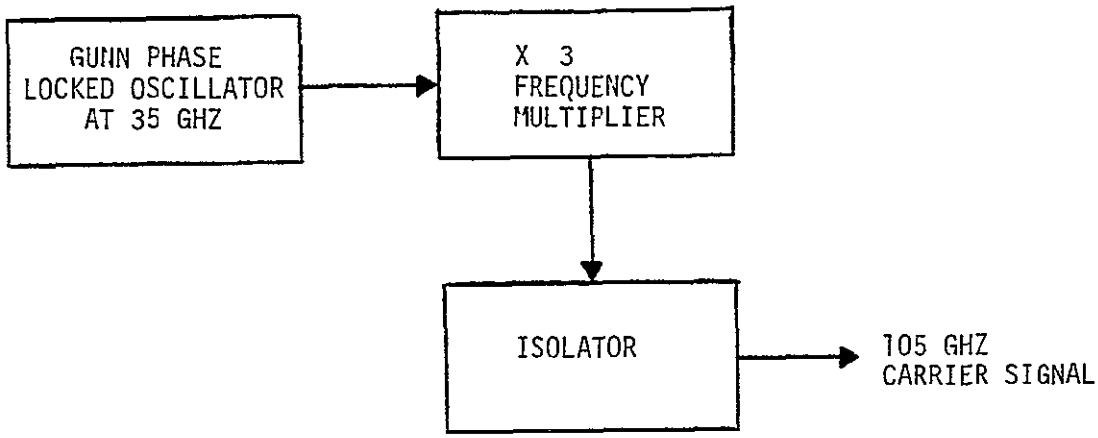


FIGURE 14: FREQUENCY MULTIPLIER CHAIN

This type of technique can be used only to 100 GHz and would be very expensive to implement for a demonstration unit.

The best choice for improving the source appears to be that of using frequency multiplying techniques which can generate millimeter wave signals from low frequency power sources. A 35 GHz phase locked Gunn oscillator can be used as the input to a x3 frequency multiplier to generate a ultra-stable low noise 105 GHz carrier signal. The Gunn oscillator can be phase locked to a crystal source with a power output of up to 100 mW. This would give a power output from the frequency multiplier of 10 mW. This method holds the promise of increasing the range while decreasing the phase noise of the demonstration unit. Although this method would be moderately expensive to implement it appears to be the most feasible method of generating a low noise ultra-stable source above 100 GHz. Figure 14 shows a block diagram of a 105 GHz multiplier chain.

The UCS system could also be improved by choosing a larger antenna. By using a 18 inch parabolic antenna instead of a 6 inch one, the gain can be improved to 51 dB from 42 dB (at the expense of larger system size). This would increase the range of the system considerably. (The 6 inch antenna was chosen for lower cost and to demonstrate the effectiveness of using a parabolic antenna.)

By replacing the harmonic mixer with a balanced mixer - IF preamp, replacing the Gunn oscillator with a stabilized frequency source, and using 18 inch parabolic antennas instead of the smaller 6 inch ones the range could be improved to a theoretical limit of 45 km. Such a unit would still be far from capable of meeting the promise of space-use for an ultramicrowave communications system, however. In particular, advances in millimeter wave component integration techniques, reliability, and producibility are required.

APPENDIX A

OPERATION OF THE ULTRAMICROWAVE COMMUNICATIONS SYSTEM

This appendix covers the procedures to make the Ultramicrowave Communications System operational. This includes procedures required for maintaining compatibility between individual subsystems, as well as tuning and alignment procedures.

a) Operation of the ADCMS and DDACS

The A/D Converter Multiplexer Subsystem (ADCMS) and Demultiplexer D/A Converter system (DDACS) are designed to be compatible with the transmitter and receiver of the Ultramicrowave Communications System. The output of the ADCMS is compatible with the input of the transmitter and the input of the DDACS is compatible with the output of the receiver. The ADCMS and DDACS were also designed to be compatible with each other. This is very convenient, as the two can be connected together to ensure they are operating properly. Photo A1 shows the units in front view, and Photo A2 shows the rear view of the units. This section describes the procedure required for ensuring compatability between the individual subsystems as well as describing performance tests of the ADCMS and DDACS when operating in tandem.

The ADCMS interfaces two video signals, with frequency components up to 5 MHz, to the input of the transmitter. These two signals are input to the ADCMS at the ports labeled "VIDEO 1" and "VIDEO 2". The inputs are configured to an input impedance of 75 Ω and can accept a maximum 1 volt peak-to-peak analog signal. Input impedance and dynamic range can altered by changing resistor values

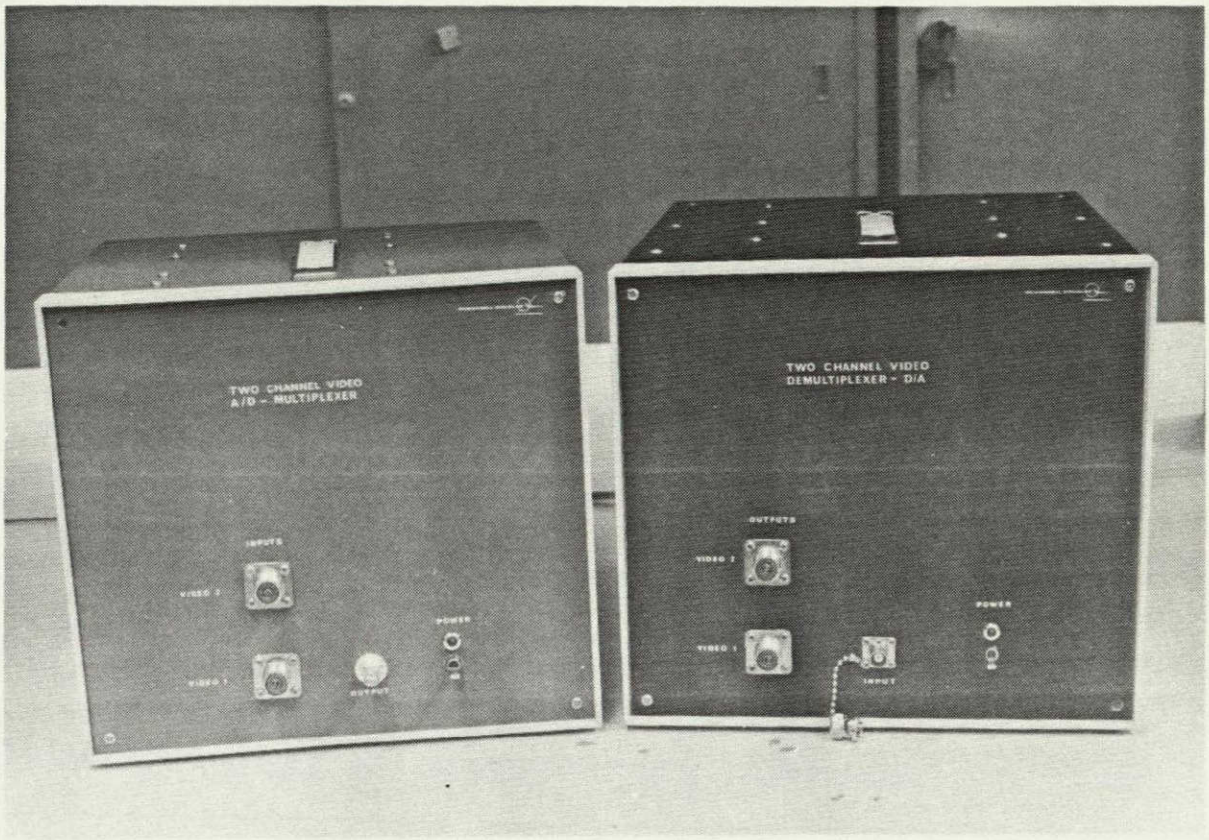


Photo A1 Front View of ADCMS (left) and DDACS (right).

on the A/D converter boards (see Appendix G). Trimming potentiometers are provided on the A/D converter boards to adjust the DC offset and gain of the input buffer amplifiers (see Appendix G). In use the input signal lines should be 75Ω, such as RG-59. The input connectors are type UHF female jacks.

The output of the ADCMS is a 130 Mb/second bit serial stream in a non-return-to-zero (NRZ) format.

The output is emitter coupled logic (ECL) levels and is unterminated. In use, the output signal line should be 50Ω, such as RG-58 coaxial cable, and should be terminated in 50Ω to -2 volts, to prevent reflections. When used as the input to the transmitter of the UCS, an external termination is not

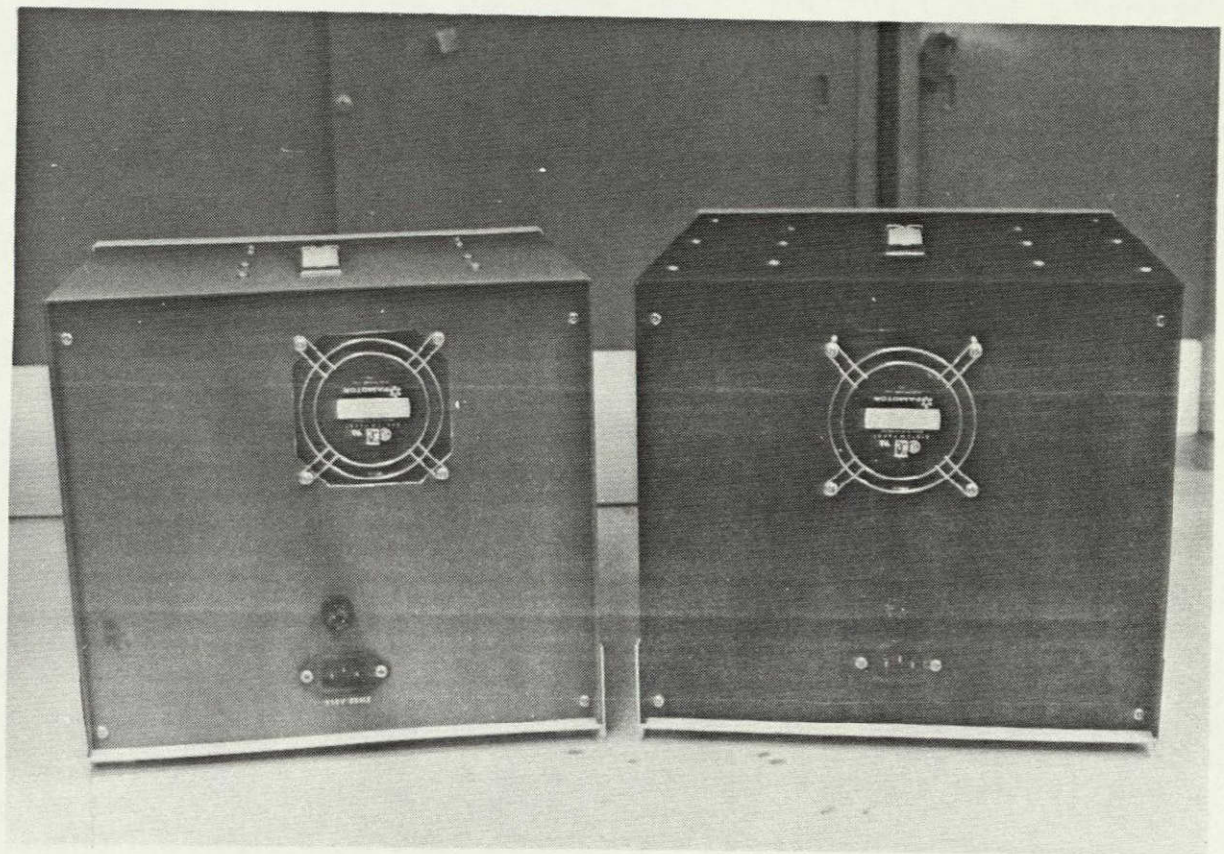


Photo A2 Rear View of ADCMS (left) and DDACS (right).

required. The length of any output cable should be held to 50 feet or less to prevent degradation of the signal. The output connector of the ADCMS and the input connector of the transmitter are type BNC female jacks.

The DDACS interfaces the output of the receiver with the input of two video monitors. The input of the DDACS accepts an ECL level digital signal. It is terminated with 50Ω to -2 volts, and it is recommended that 50Ω coaxial cable be used to supply the data. The input connector is a type BNC female jack.

The outputs of the DDACS are 0-5 MHz video signals. Each output channel has 75Ω impedance, and is capable of supplying 1 volt peak-to-peak unloaded, or .5 volt peak-to-peak to a 75Ω load. The output signal levels are between 0 and -1 volt unloaded, or 0 and -.5 volt when driving a 75Ω load. It is recommended that 75Ω coaxial cable be used to supply the output signals to video monitors. The outputs are labeled "VIDEO 1" and "VIDEO 2", corresponding to the input jacks of the ADCMS. In use, the video signal at "VIDEO 1" of the ADCMS will be output at the "VIDEO 1" terminal of DDACS, and similarly for the "VIDEO 2" terminals. The output connectors are type UHF female jacks.

Before being used with the UCS transmitter and receiver, the ADCMS and DDACS should be operated in tandem to ensure they are working properly. Special note should be made of offset and gain adjustments on the A/D boards. These will usually require adjustment whenever a new video source is used to compensate for the dc offset and signal level variations between sources. This is most easily accomplished by a setup as in Figure A1, but using the video source instead of a signal generator, and adjusting the offset and gain adjustments until the output is an accurate representation of the input. If the signal level from the video source is too high to be compensated for by the gain adjustment, it is helpful to use a variable attenuator between the output of the video source and the input of the ADCMS.

If the ADCMS and DDACS are used with the Ultramicrowave Communication System transmitter and receiver, correct synchronization may be difficult to obtain unless a video source is present at each of the two inputs. The reason for this lies in the way the DDACS recognizes the sync bit. The DDACS looks for a non-changing low bit; if it finds one it is assumed to be the synchronization bit.

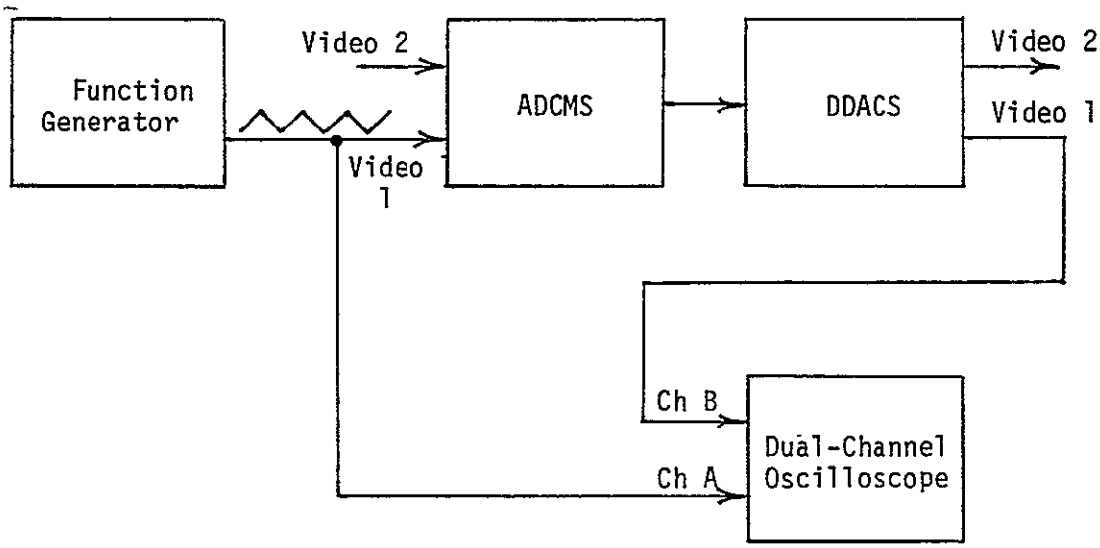


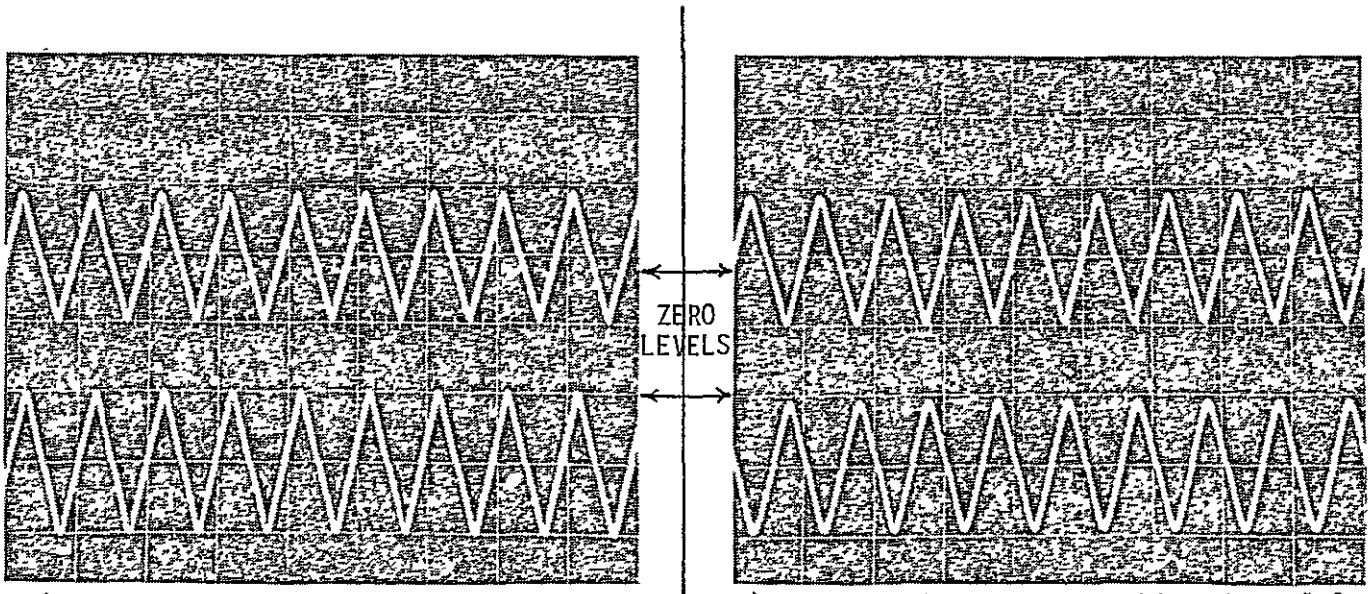
Figure A1. Setup to Test Performance of ADCMS and DDACS with Triangle Wave Input

Since there exists a 180° ambiguity in demodulated bi-phase data, these constant highs may be output by the receiver as constant lows which could be mistaken for sync bits. The DDACS is able to resolve the ambiguity and correctly synchronize only if signals are present on both video channels, so that the only nonchanging data bit will be the synchronization bit. It is recommended, therefore, that video signals be present on both channels if used with the ACDMS and DDACS.

As a demonstration of the ability of the ADCMS and DDACS to transmit a signal without degradation, a triangle wave was used as a test signal. The ADCMS and DDACS were connected as shown in Figure A1, and the test signal was introduced into video input 1. Video input 2 was left open. The signal, after pass-

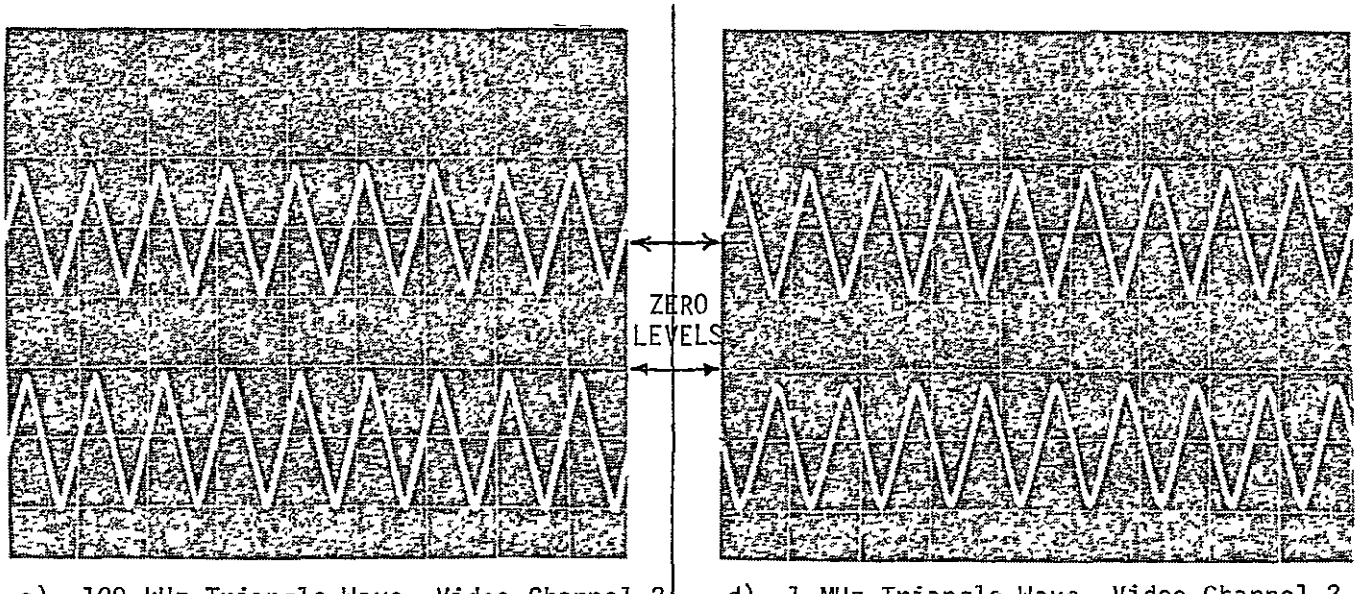
ing through the ADCMS and DDACS to video output 1 was compared to the input signal on an oscilloscope. Figure A2a compares the input and output signals for a 100 kHz traingle wave. Figure A2b makes the comparison for a 1 MHz triangle wave. Similarly, Figures A2c and A2d show the response of video channel 2 to 100 kHz and 1 MHz triangle waves, respectively. The photos show the dc offset on the input signal (this is adjustable), and the fixed dc offset on the output signal. For the 100 kHz signals, the output signal is a very good representation of the input. A small amount of rounding is evident at the corners of the 1 MHz signal. This is due to the finite bandwidth of the A/D and D/A converters, and to the 5 MHz low pass filters on the outputs of the DDACS. The output signal is still quite a good representation of the input signal, however.

The ultimate test of the ADCMS and DDACS is their ability to operate on actual video (i.e., television) signals. Video signals supplied by a video camera were fed to a video monitor and to the video input 1 of the ADCMS. Video input 2 was left open. The output of the ADCMS was connected to the DDACS, and the resulting Video 1 output fed to a second video monitor for comparison with the input signal. Figure A3 shows the setup. Figure A4 is a photo of two video monitors. The monitor on the left shows the video picture input to the system, while the monitor on the right shows the picture after passing through video channel 1 of the ADCMS and DDACS. The pictures are nearly identical, indicating that very little degradation in signal quality has occurred. Similarly, Figure A5 shows the results of the video picture passing through video channel 2. Once again the pictures are nearly indistinguishable, indicating that the video quality is quite high.



a) 100 kHz Triangle Wave, Video Channel 1
10 μsec/Horizontal Division

b) 1 MHz Triangle Wave, Video Channel 1
1 μsec/Horizontal Division



a) 100 kHz Triangle Wave, Video Channel 2
10 μsec/Horizontal Division

d) 1 MHz Triangle Wave, Video Channel 2
1 μsec/Horizontal Division

Figure A2. Results of Performance Test of ADCMS and DDACS
(Upper Trace: input to ADCMS)
(Lower Trace: output of DDACS)
(All Photos 1 Volt/Vertical Division)

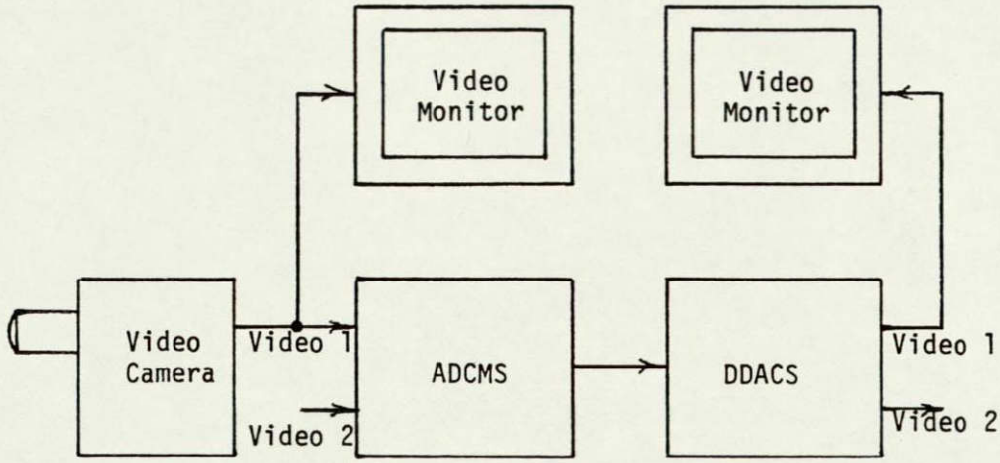


Figure A3. Setup to Test Performance of ADCMS and DDACS with Video (Television) Signal Input

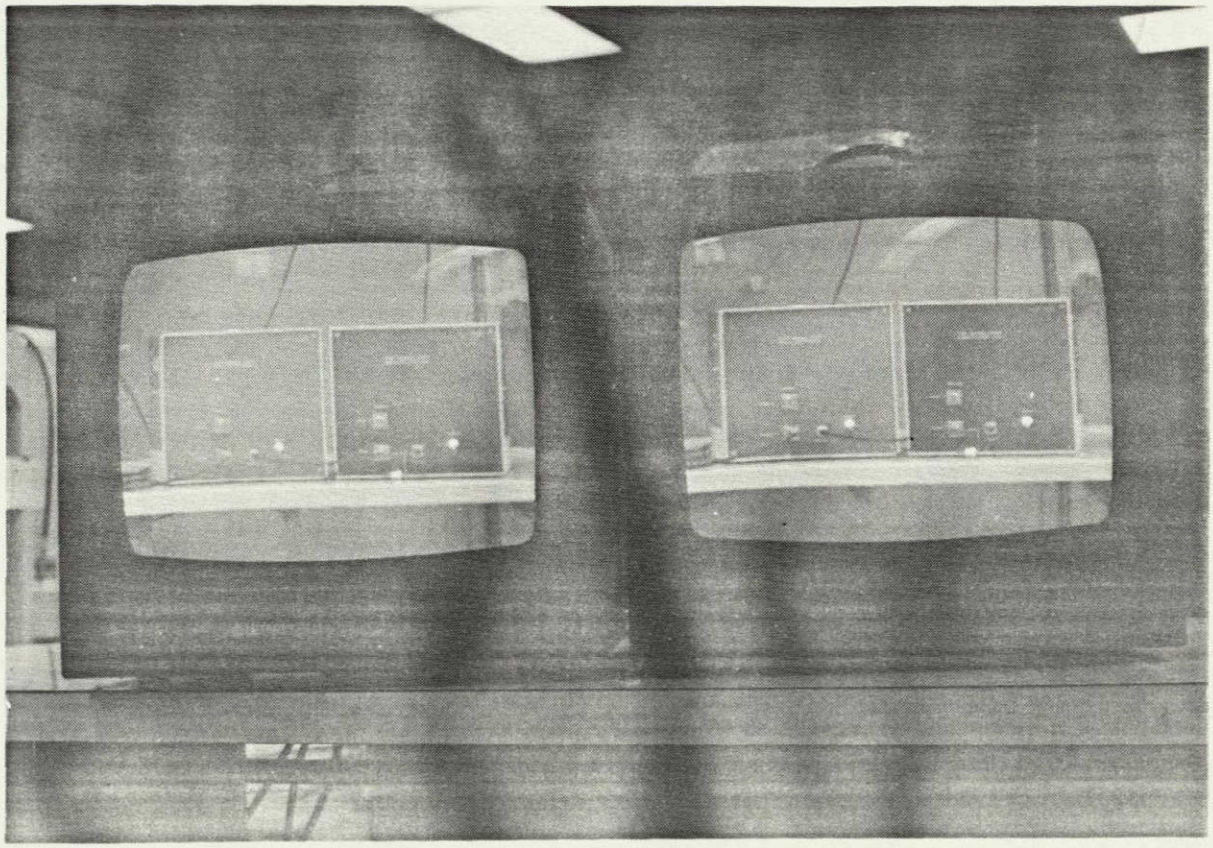


Figure A4. Comparison of Video Picture Quality for Video Channel 1.
left: input video picture
right: output video picture

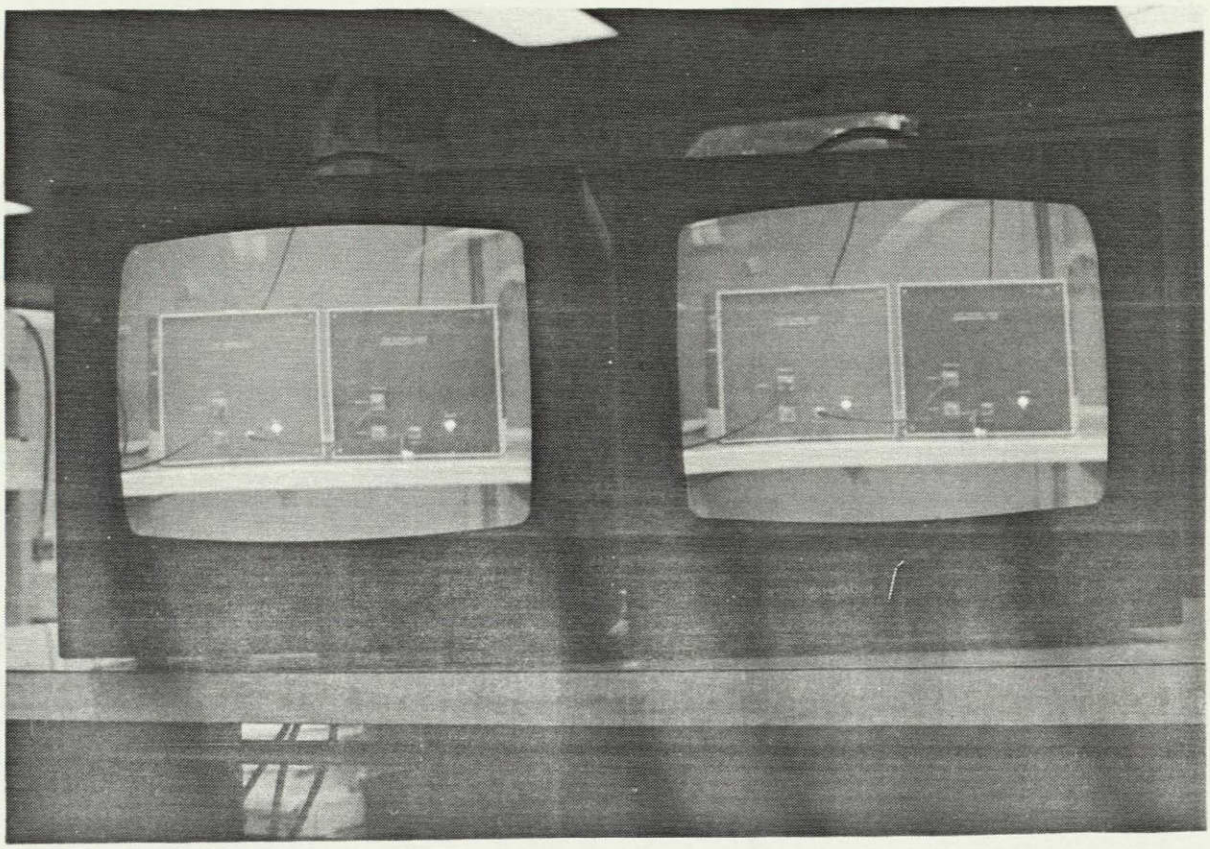


Figure A5. Comparison of Video Picture Quality for Video Channel 2.
left: input video picture
right: output video picture

Whenever the ADCMS and DDACS are connected directly together, as in Figures A1 and A3, it is sufficient to use only one of the two video channels; the other can be left open. If correct synchronization is not obtained immediately, it can usually be obtained quite easily by turning the DDACS off and then back on again.

b) Operation of the Transmitter and Receiver

The UCS is designed to transmit and receive a 130 Mb/sec bit serial information stream at a carrier frequency of 105 GHz. The UCS is completely compatible with the ADCMS and DDACS subsystems. However, to ensure proper operation, the UCS may be operated as a stand-alone system (i.e. with no information being transmitted). This section describes procedures for properly aligning and tuning the UCS, as well as interfacing and connection requirements.

The transmitter of the UCS can accept a serial digital input signal with frequency components to 130 MHz. The input is configured for 50Ω input impedance and a 1 volt peak to peak ECL level signal (-1 to -2 volts). The input is terminated with 50Ω to -2 volts, so external terminations are not required. In use the input signal line should be 50Ω coaxial cable such as RG-58. The input connector is a type BNC female jack.

The output of the UCS receiver is the transmitted digital data stream. The output channel is capable of supplying this signal at a 130 Mb/sec rate, at ECL levels. The output port is configured for 50Ω output impedance and is unterminated. When used with the DDACS, the output signal line may be connected directly to the input of the DDACS with no external terminations. In use it is recommended that the output signal line should be 50Ω coaxial cable such as RG-58. The other three ports of the receiver (IF output, demodulator input, error signal output) are also nominally configured for 50Ω output impedance. The IF output and demodulator input ports are provided for diagnostic purposes. In use the IF output may be connected directly to the demodulator input via a short piece of RG-58 cable. The error signal output port is purely for diagnostic purposes. The connectors are all type BNC female jacks.

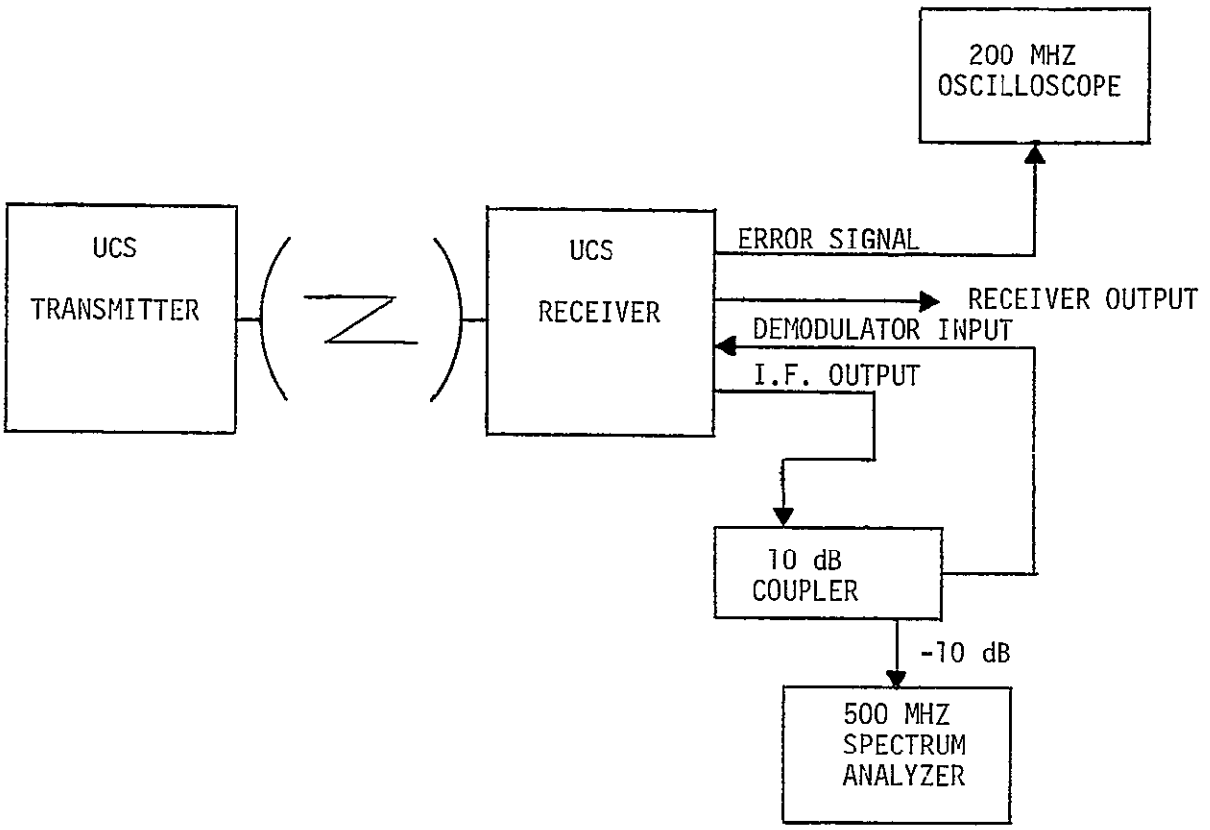


FIGURE A6; SETUP TO TUNE AND ALIGN THE UCS SYSTEM

The best method of initially tuning the receiver to the transmitter appears to consist of tuning the receiver directly to the carrier signal. This can be accomplished by using the UCS with no input signal.

Figure A6 shows a setup for tuning. The spectrum analyzer should have a frequency range of up to 500 MHz. The oscilloscope should be able to resolve frequencies up to 200 MHz, and can best be used on the .1 volt setting with a 50Ω feed through to the input. A range of about 30 feet is satisfactory for initial tuning.

Both the transmitter and receiver should be allowed to warm up for approximately 20 minutes before using, to allow the oscillators to stabilize. The IF output of the receiver should be a single spike around 273 MHz. If the signal cannot be detected it can usually be obtained by turning the transmitter off, then back on again. The coarse adjustment on the receiver can be used to center the IF output at 273 MHz. The fine tune knob can then be adjusted until the error signal is a constant voltage (see Appendix C for more detail). This indicates that the demodulator is locked to the IF frequency. The antennas should be aligned to obtain a maximum signal level on the spectrum analyzer.

Once the UCS has been tuned and aligned, the spectrum analyzer and oscilloscope may be removed. The fine and coarse tune knobs will need periodic adjustments due to the drift of the millimeter wave oscillator.

When used with the ADCMS and DDACS subsystems, special attention should be paid to the adjustments on the video sources used. Aperture, focus, beam strength, and output attenuation are critical camera settings for transmitting a quality video signal.

APPENDIX B

DETAILED DESCRIPTION OF TRANSMITTER SYSTEM

A block diagram of the transmitter was shown in Figure 4. It showed that the transmitter is composed of four major functional blocks, the parabolic antenna, RF subsystem, modulator driver, and power supply subsystem. This section describes each of these functional blocks in more detail, including schematics and layout drawings as well as discrete performance analysis.

a) Antenna

The antenna chosen was a Alpha/TRG model number 802-6, 6 inch parabolic antenna. This antenna has a machined aluminum casting reflector for optimum performance at upper frequencies. These reflectors have typical surface tolerances of .001 inches RMS. The reflector feed consists of a section of standard W-band wave guide, which has been end flared for optimum reflector illumination. Input signals are connected to the feed at a standard rectangular wave guide flange. Appendix F shows a layout of the antenna feed system.

The antenna was designed for a center frequency of 104.725 GHz. Bandwidths were given as nominally ±5%. This is a large enough bandwidth to compensate for drift in the millimeter wave oscillator. Gain was found from $G = N\left(\frac{\pi D}{\lambda}\right)^2$ where N = .55, D is the antenna diameter and λ is the center frequency wavelength. For our case this gives a gain of 42 dB. Half power beamwidth is found from $\theta\ 1/2 = 70\ \frac{\lambda}{D}$. The θ 1/2 for a 6 inch antenna is found to be 1.36°, which agrees with the experimental results as found on the antenna pattern charts. Side lobes are nominally -22 dB. The antenna beam is vertically polarized by the wave guide feed.

b) RF Subsystem

The RF subsystem of the transmitter accepts the digital information from the modulator driver and produces the high frequency bi-phase modulated signal. The

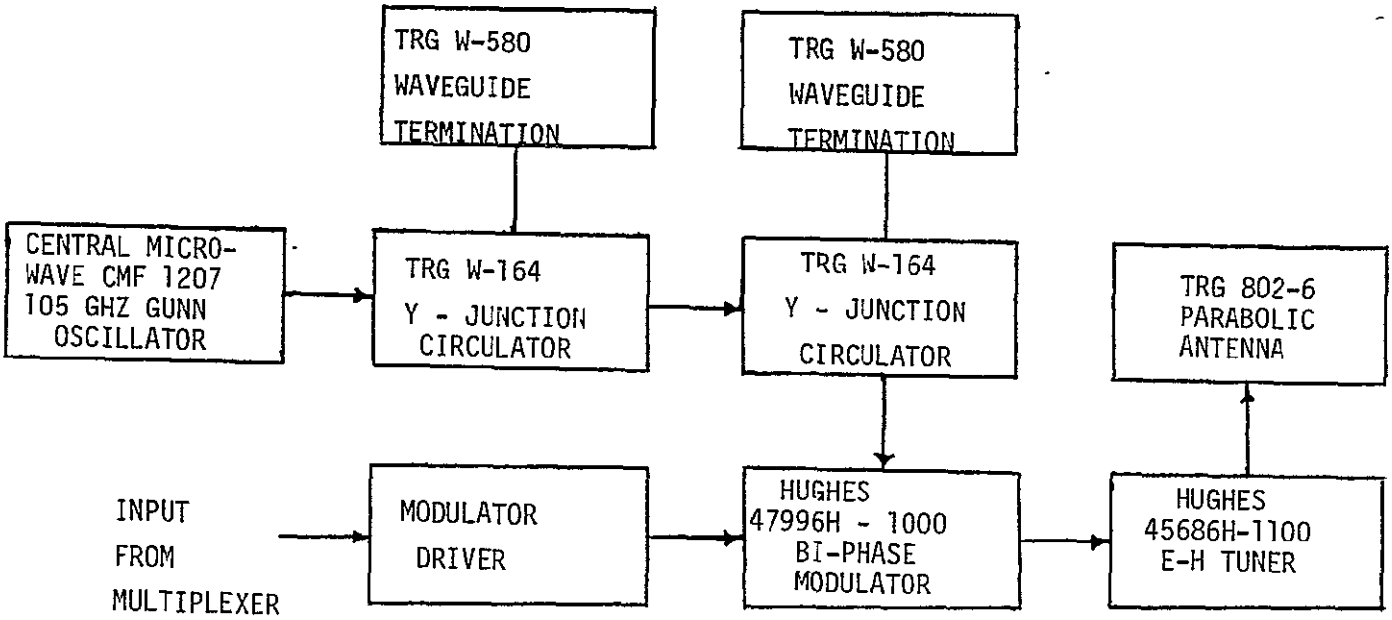


FIGURE B1; TRANSMITTER SYSTEM

RF design includes nonactive components in order to improve the performance capability of the system. A detailed diagram of the RF subsystem, along with its relation to the modulator driver and antenna, is shown in Figure B1.

The millimeter wave source chosen is a Central Microwave, model number 1207, mechanically tunable Gunn oscillator. The center frequency is 104.725 GHz and is tunable over a range of ±100 MHz. Tuning is achieved by adjusting the screw located on top of the oscillator. Power supply requirements at 104.725 GHz were found to be +4 Vdc at .25A. Power output of the source is 5 mW. This gives an oscillator efficiency of .001%. Output frequency can also be adjusted by varying the input voltage over the allowable limits. Appendix F gives a manufacturers data sheet of specifications.

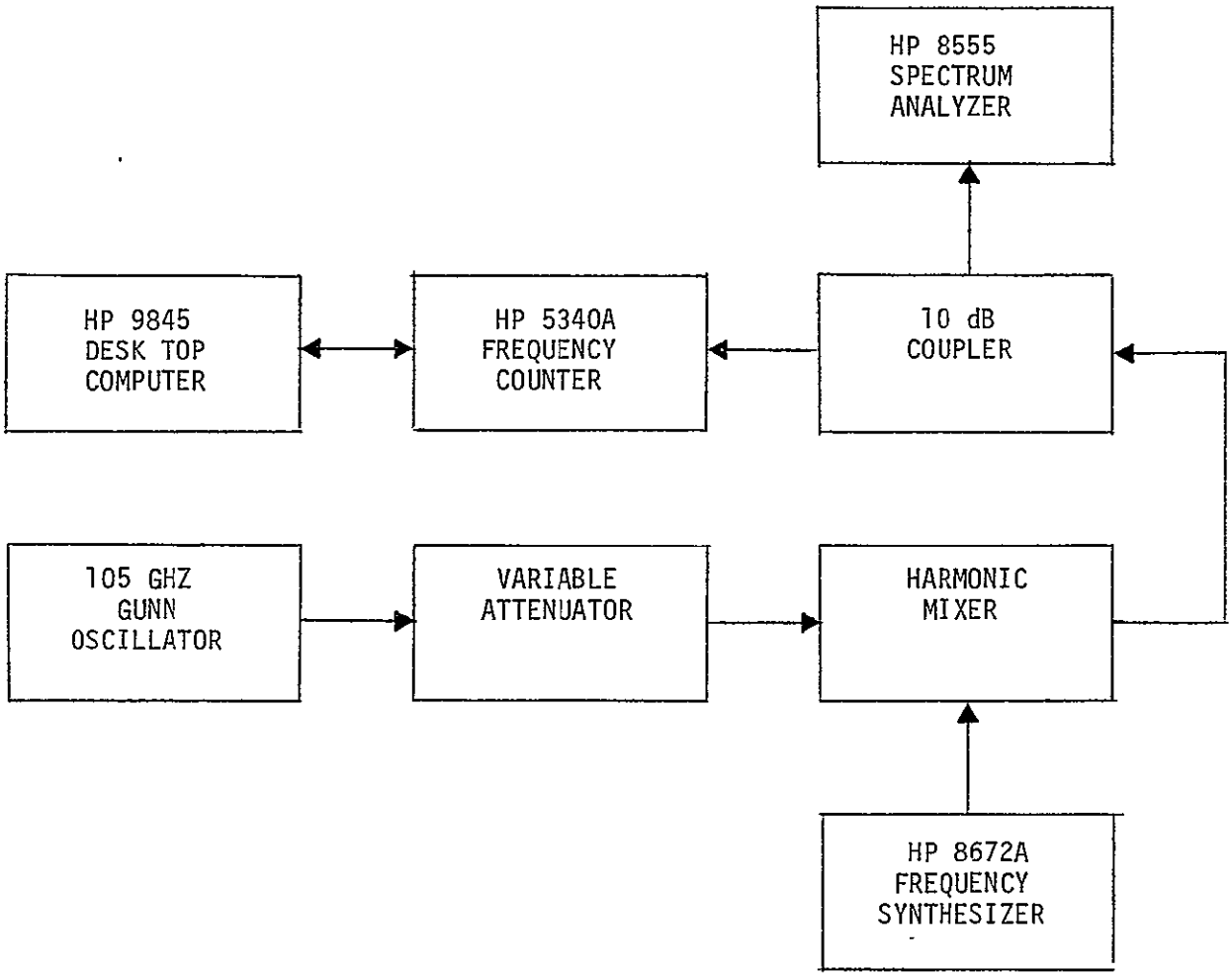


FIGURE B2; FREQUENCY MEASUREMENT SETUP

Since the oscillator is used in a free running mode, it was necessary to make measurements of its frequency stability so that the receiver could be designed accordingly. Frequency variations were measured by a setup as shown in Figure B2. Using this method, plots of frequency deviation versus time were made, from which an average drift rate and peak-to-peak frequency deviations were found.

Initial measurements showed severe frequency instabilities in the millimeter wave oscillator. These frequency changes can be attributed to several operating conditions. First, variations in the applied dc potential will certainly alter the frequency. The tuned resonant frequency of the cavity can be altered by thermal expansion of various parts, changes in air pressure, and by mechanical vibrations. Also, variations in load impedance, resulting in both resistive and reactive components, cause changes in frequency. Finally, changes in ambient temperature critically affect the frequency of oscillation.

To compensate for changes in the applied potential, the output of the power supply was low pass filtered to reduce transients and give a stable dc voltage. Mechanical vibrations were reduced, as well as stabilizing the ambient temperature, by securely mounting the oscillator on a heat sink. Changes in load impedance were compensated for by isolating the oscillator from the load.

Using these improvements, measurements were made of frequency deviation versus time for both long and short term intervals. Figure B3 shows frequency measurements taken over a period of 1.02 secs. This graph shows a sinusoidal drift of the oscillator about an average frequency of 104.602 GHz. This drift is cyclic at a rate of approximately 10 Hz/sec with a peak to peak frequency variation of 60 kHz. Frequency changes over such a short time period can be considered as localized drift about a fluctuating average frequency. This small localized drift is not as critical to the design of the receiver as is the long term drift. (The receiver has to be able to track large changes in frequency in order to remain in lock with the transmitter.)

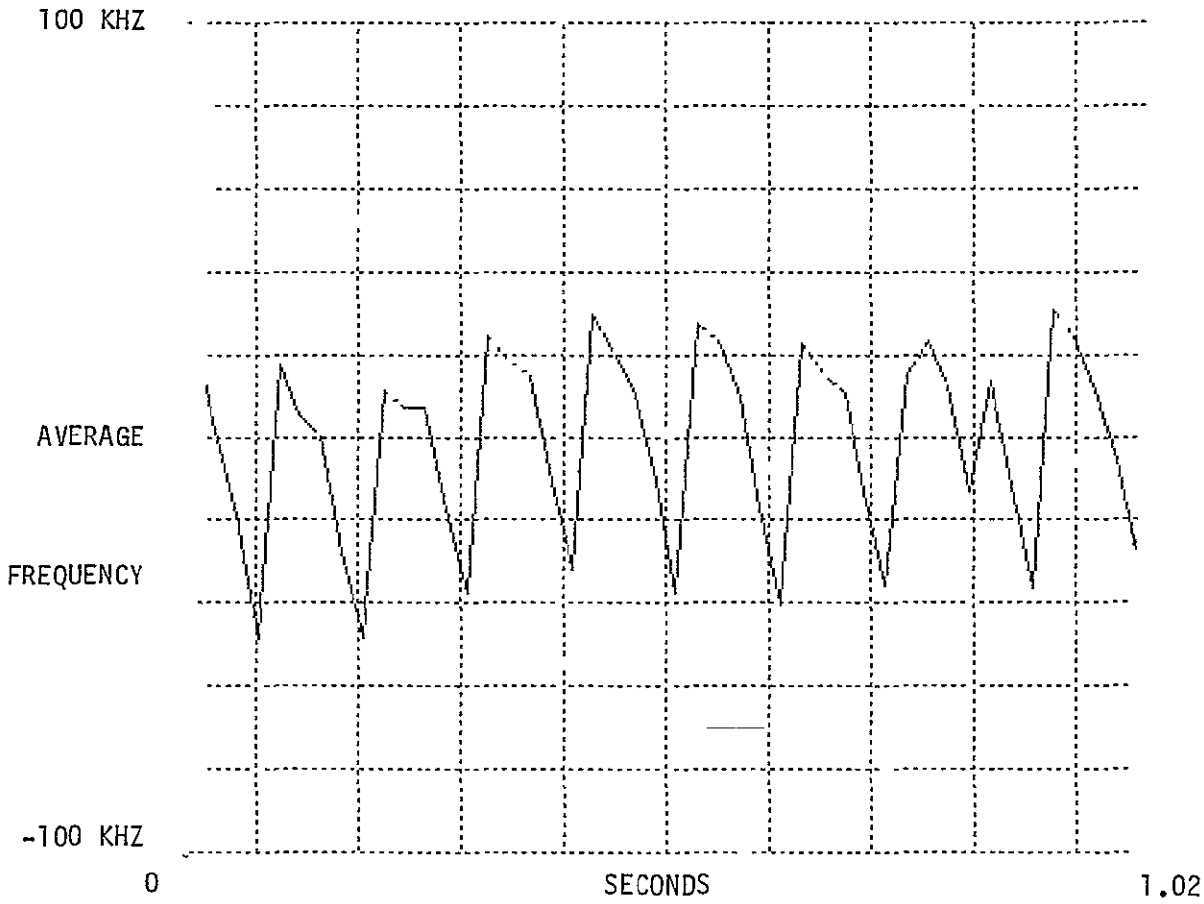


FIGURE B3; SHORT TERM MEASUREMENT OF FREQUENCY DRIFT.

.0204 SECONDS/MEASUREMENT

1 KHZ RESOLUTION

AVERAGE FREQUENCY = 104.602 GHZ

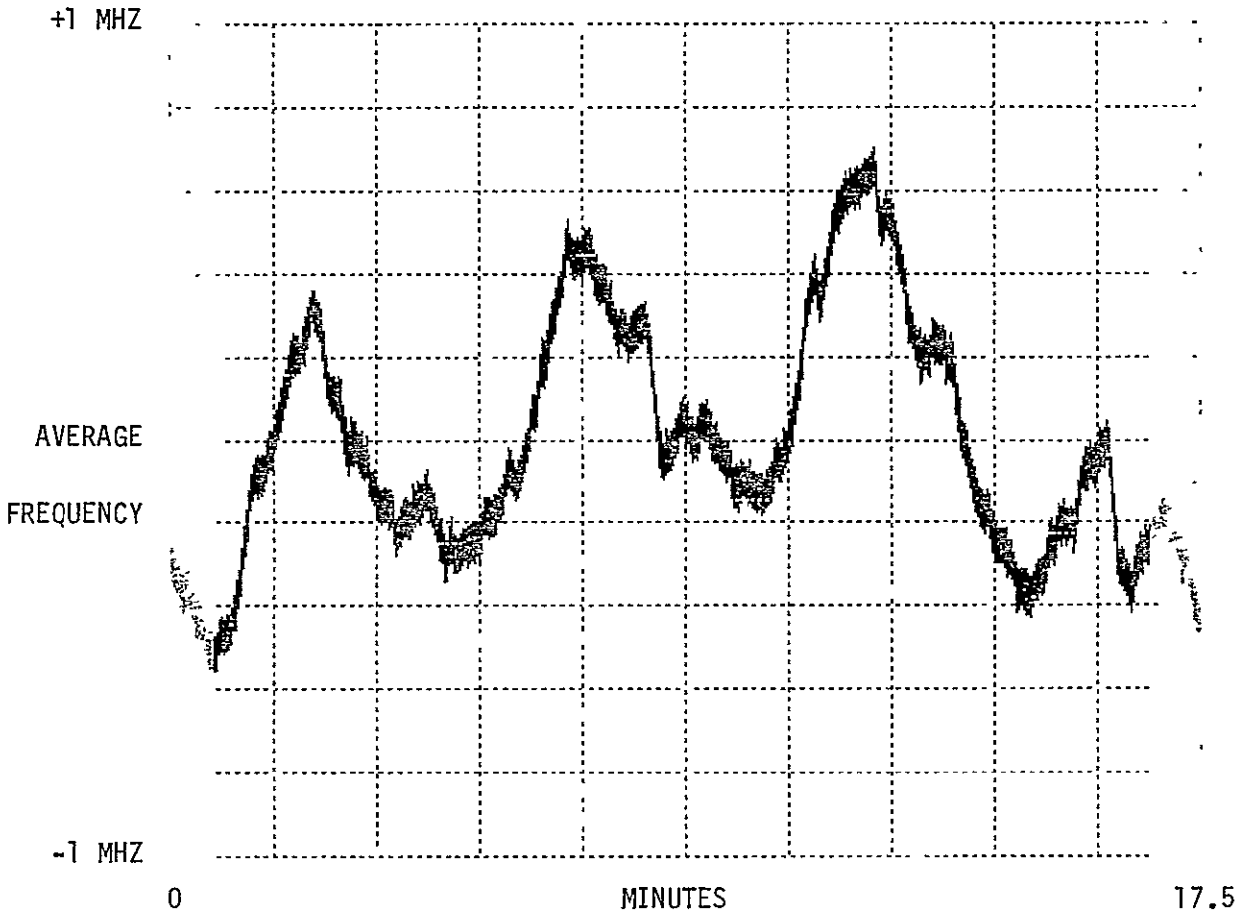


FIGURE B4; LONG TERM MEASUREMENT OF FREQUENCY DRIFT

.105 SECS/MEASUREMENT

1 KHZ RESOLUTION

AVERAGE FREQUENCY = 104.610 GHZ

Figure B4 shows measurements taken over a period of 17.5 minutes. This chart again shows a sinusoidal drift of the oscillator about a mean frequency. The average is 104.610 MHz. Minimum long term drift rates of approximately 1 MHz/minute were observed. This large, long term drift is the frequency change that the receiver needs to be able to track in order to remain in lock with the transmitter.

Although this oscillator shows severe instability characteristics, it still has better performance capabilities than the originally chosen IMPATT oscillator. Even though the IMPATT showed the promise of higher power output, (approximately 50 mW), the stability characteristics were much worse than those of the Gunn, and the life-time was extremely short.

The output of the oscillator is fed into two circulators, which act as isolators from a possible load mismatch with the bi-phase modulator. The circulators are Alpha/TRG series 164 E-plane 3-port devices. Circulation between ports is in the order of 1-2, 2-3, and 3-1. Isolation in the opposite direction is nominally 20 dB. These circulators are used as isolators by inputing RF energy into port 1 and taking the output on port 2. Reflections from the load appear at port 3 which is terminated with a wave guide load. Thus, reflected power is absorbed by this load and does not appear at port 1. Connecting two of these devices in series provides sufficient isolation of the oscillator from the load.

This RF signal is input to the modulator for modulation by the digital data. This is a Hughes 47996H-1000 PIN bi-phase modulator. It is a circulator coupled, path-length modulator that provides a 0° or 180° phase shift to the RF signal, depending on the state of the PIN diode. The method of operation involves using the variable capacitance of the PIN diode. The diode cavity is adjusted at a mean biasing point so that parallel resonance is achieved. The diode is then switched between on and off states by the digital information from the modulator driver. This alters the effective path length of the signal through the 2nd arm of the circulator by half a wave length, thus producing a phase shift about the resonant frequency. The bi-phase modulated signal is then output from the third port of the circulator. Appendix F contains a manufacturers data sheet of the bi-phase modulator.

Before the signal is transmitted from the parabolic antenna, a tuner is used for impedance matching between the modulator and the antenna. This is a Hughes 45686H-1000 E-H plane tuner. It consists of a hybrid tee, in which micrometer tuned adjustable shorts are placed in the series and shunt arms. The effect of these shorts is to produce shunting reactances in both the E and H planes thus altering the phase and amplitude of the reflection coefficient. The tuning stubs were adjusted until a maximum signal level was detected from the output of the antenna. (This implies that the reflection coefficient from the antenna was at a minimum amplitude and proper phase.)

c) Modulator Driver

The modulator driver circuit is designed to provide the proper "on" current (10 mA) and "off" voltage (10 volts) to the PIN diode load of the bi-phase modulator. It is capable of switching between states at a rate of 130 MHz. The circuit accepts the digital information from the ADCMS, and then switches the diode of the modulator either "on" or "off" according to the state of the information. The diode is on for a binary 0 and off for a binary 1. Figure B5 shows a schematic of the modulator driver circuit. Appendix G contains a parts list for the circuit.

The ECL serial output from the multiplexer is input to the modulator driver through a 100101 Or/Nor gate. The Or output drives the base of transistor B of the differential amplifier, and the Nor output drives the base of transistor A. In operation there are two different cases to be considered.

The first case is when the input is a logic zero. The Or output of the 100101 is -2 volts and the Nor output is -1 volts. This has the effect of turning on transistor A and turning off transistor B. Hence the emitter current of B

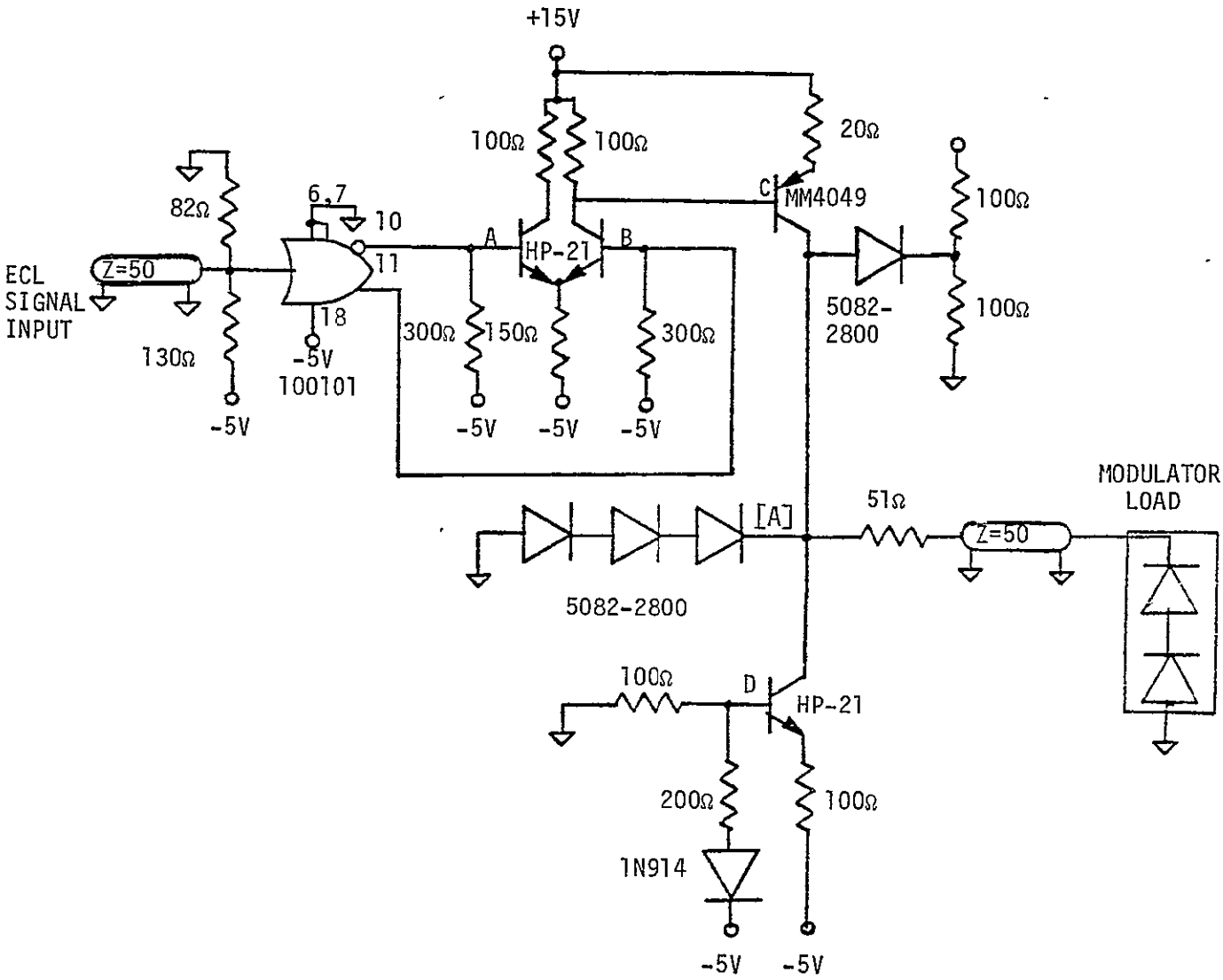


FIGURE B5; MODULATOR DRIVER CIRCUIT

is zero, which implies that the collector voltage of B is also equal to zero. This in turn causes the input voltage on the base of transistor C to be zero. When this happens no output current appears at node A from the collector of C. Transistor D is biased in such a manner as to act as a constant current source that draws 28.7 mA from node A. For the case being considered, this 28.7 mA is drawn from the three 5082-2800 diodes in series and from the load. It is found that the diodes input 20.9 mA to node A, which causes the load to input 7.8 mA.

This is the "on" current of the bi-phase modulator, which is seen to be well under the maximum rating of 10 mA.

The second case to be considered is when the input to the modulator driver is a logic one. When this occurs the Or output of the 100101 is -1 volts, and the Nor output is -2 volts. These signals turn off transistor A and turn on transistor B. This causes the collector current of B to be 22 mA, and thus produces a 13 volt input level to the base of transistor C. With C biased in this manner the collector current is found to be 75 mA. Only 28.7 mA of this collector current can appear at node A, due to the constant current action of transistor D. Therefore the single 5082-2800 diode draws the remaining 46.3 mA of the collector current through the 100Ω voltage divider network. This action produces a 10 volt potential at node A. Thus it is seen that no current is drawn from either the load or the three 5082-2800 diodes. Therefore the pin diode load is in its "off" state, at a voltage level of 10 volts. This voltage level matches the manufacturers specification for the modulator.

d) Power Supply

The power supply circuit for the transmitter is shown schematically in Figure B6. The power requirement for the Gunn oscillator is +4 volts at 1.25 A. The power requirement for the modulator driver circuit is +15 volts at .15 A and -5 volts at .123A. Commercial supplies were used for all three required voltages. The +4 volts supplied to the oscillator was stabalized by the single pole low pass filter shown in Figure B6. Figure B7 shows the terminal block voltages for the transmitter power distribution.

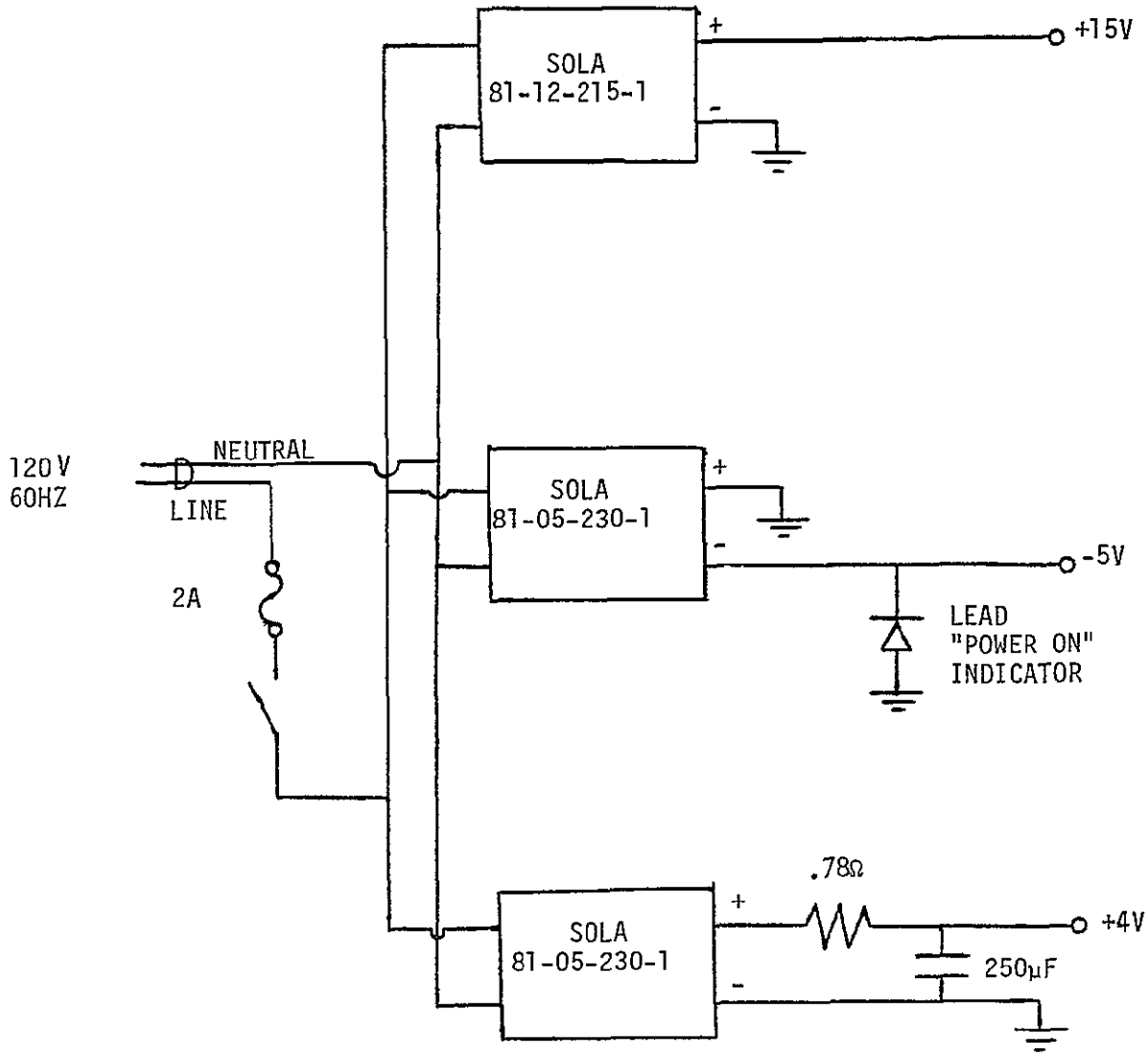


FIGURE B6; POWER SUPPLY SCHEMATIC FOR UCS TRANSMITTER

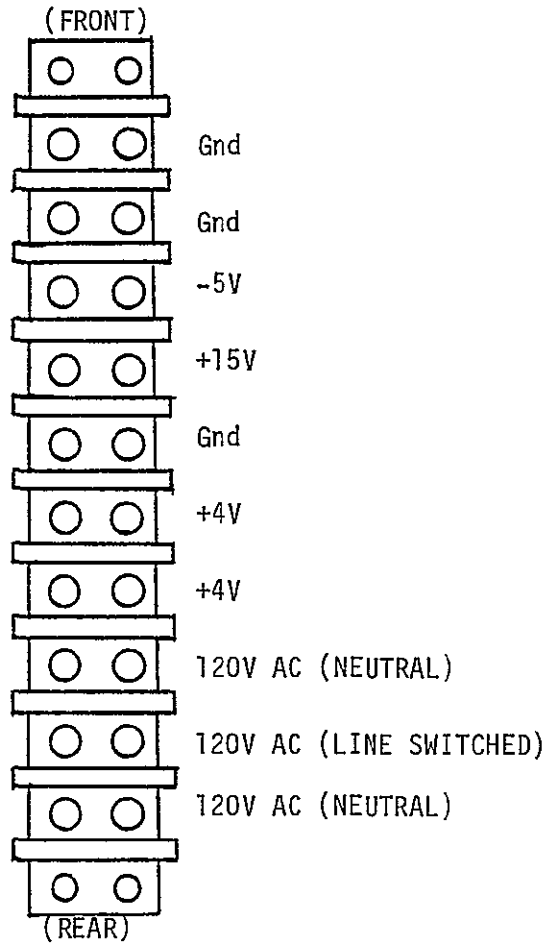


FIGURE B7: TERMINAL BLOCK VOLTAGES FOR UCS TRANSMITTER

APPENDIX C

DETAILED DESCRIPTION OF RECEIVER SYSTEM

A block diagram of the receiver was shown in Figure 7. It showed that the receiver consists of the antenna, RF front end, IF amplifier strip, demodulator, and power supply. The receiver mixes the input signal down to an IF frequency, amplifies it and demodulates it to give the original ECL bit serial stream out. This section describes each of the functional blocks in more detail, as well as individual component performance analysis.

a) Antenna

The antenna used in the receiver is the same type as that used in the transmitter. See appendix B for the details and specifications of this antenna.

b) RF Front End

The RF subsystem of the receiver mixes the incoming signal down to an IF frequency for demodulation. It consists of a 15 GHz local oscillator, two 18 dB isolators, and a harmonic mixer. Figure C1 shows a layout of these components and their relation to the other subsystems of the receiver.

The local oscillator is a Central Microwave, model number CMF520, 15 GHz Gunn diode source. This source requires an input of +8 volts at approximately 800 mA. The output power is 100 mW. This gives an efficiency of 1.6%. It has a frequency range of 12-18 GHz, and is mechanically tunable over ±100 MHz. The local oscillator is used in a free running, unstabilized mode. When the LO signal is mixed with the received signal, any frequency changes in the LO will be additive to carrier frequency changes from the transmitter. Therefore the sta-

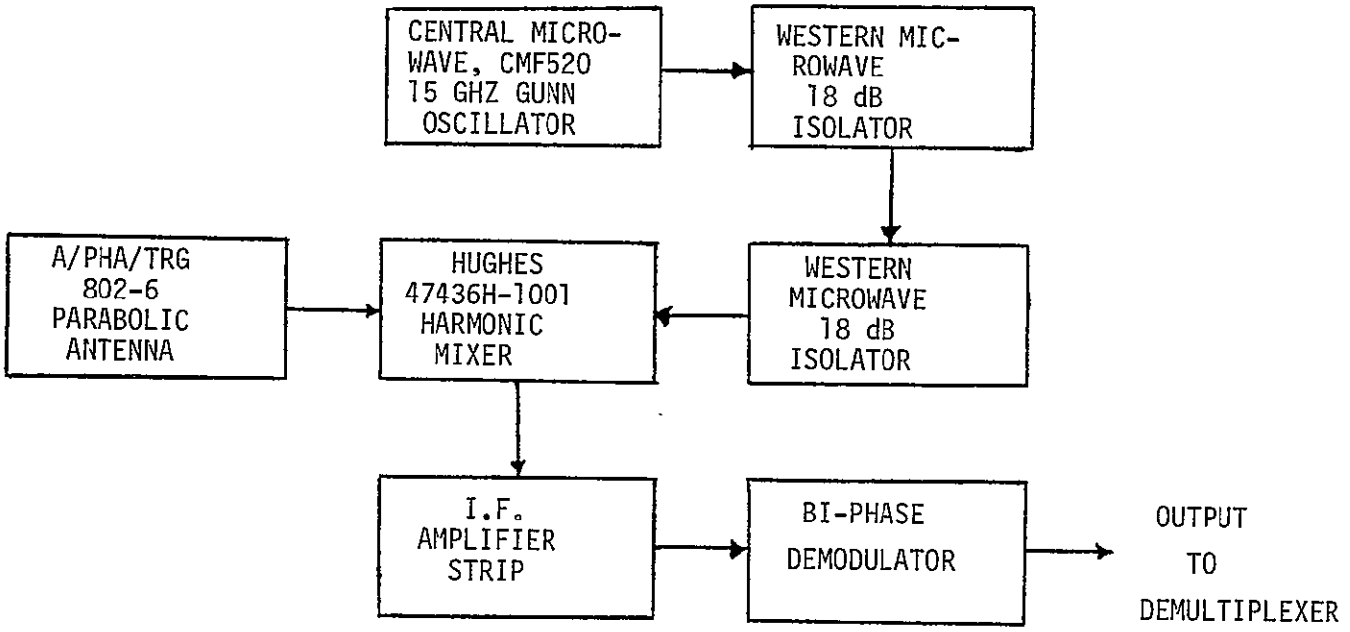


FIGURE C1; RECEIVER SYSTEM SHOWING RF COMPONENTS

bility of the local oscillator is as critical to the successful operation of the demodulator as is that of the millimeter wave source.

In order to determine the stability of the local oscillator, frequency measurements were made similar to those described in Appendix B. Before measurements were made, the oscillator was securely mounted on a large heat sink plate to help compensate for thermal and mechanical instability factors.

Figure C2 shows frequency measurements taken over a period of 100 secs. This graph shows a tendency for the frequency instability to be of a sinusoidal nature. The frequency changes at a rate of about 333 Hz/sec, about an average frequency of 15.0005 GHz. The peak to peak frequency deviation is 22 kHz. This drift can be seen as a frequency modulation of the input signal, thus producing unwanted phase noise in the system.

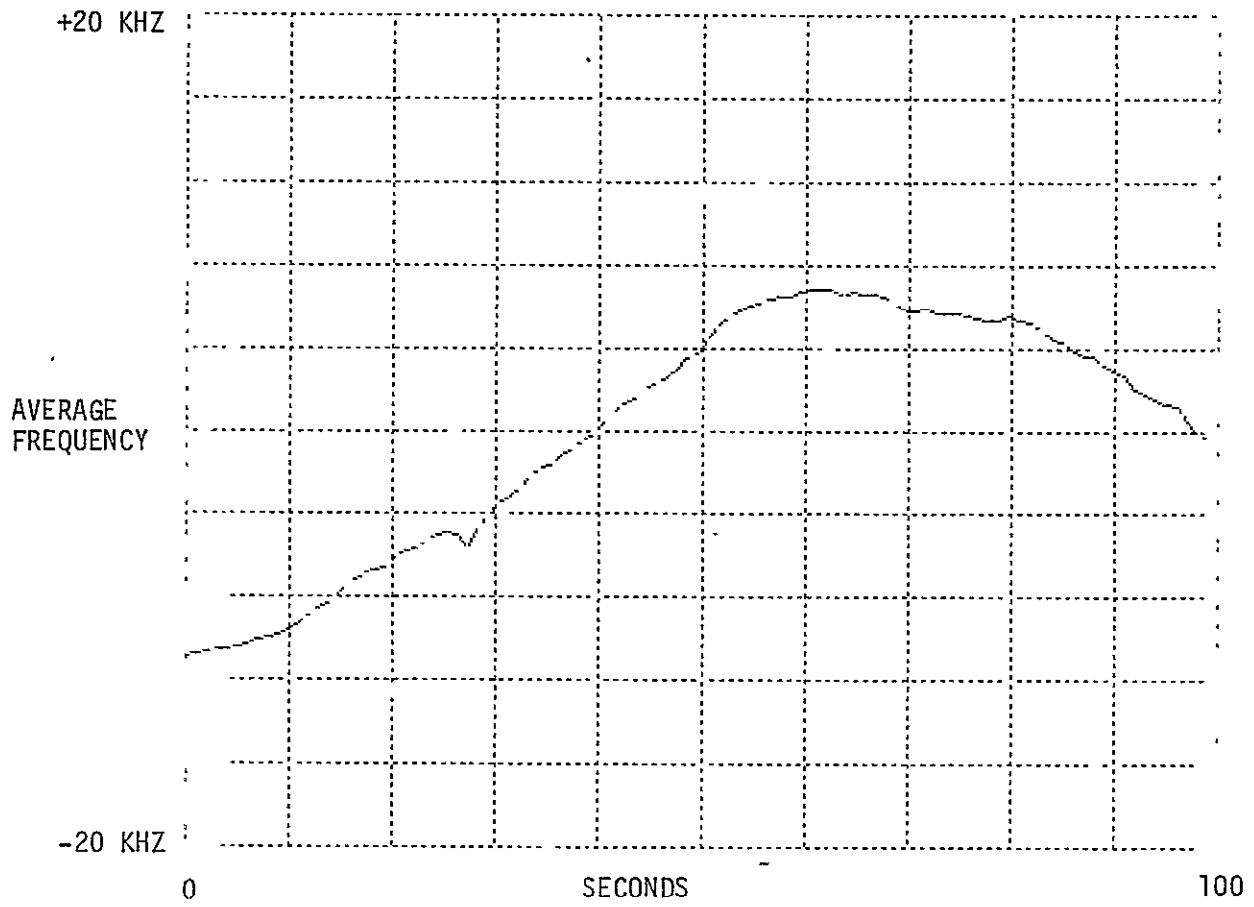


FIGURE C2; MEASUREMENT OF FREQUENCY DRIFT
1 SECOND/MEASUREMENT
100 HZ RESOLUTION
AVERAGE FREQUENCY = 15.000 GHZ

Figures C3 and C4 also show measurements taken over a period of 100 seconds. These were taken immediately after the measurements in Figure C2. As can be seen the average frequencies of these two runs are very close to that of C2. Therefore the frequency is fairly stable, with only localized deviations. Sudden discontinuities shown in the measurements are due to mechanical vibrations.

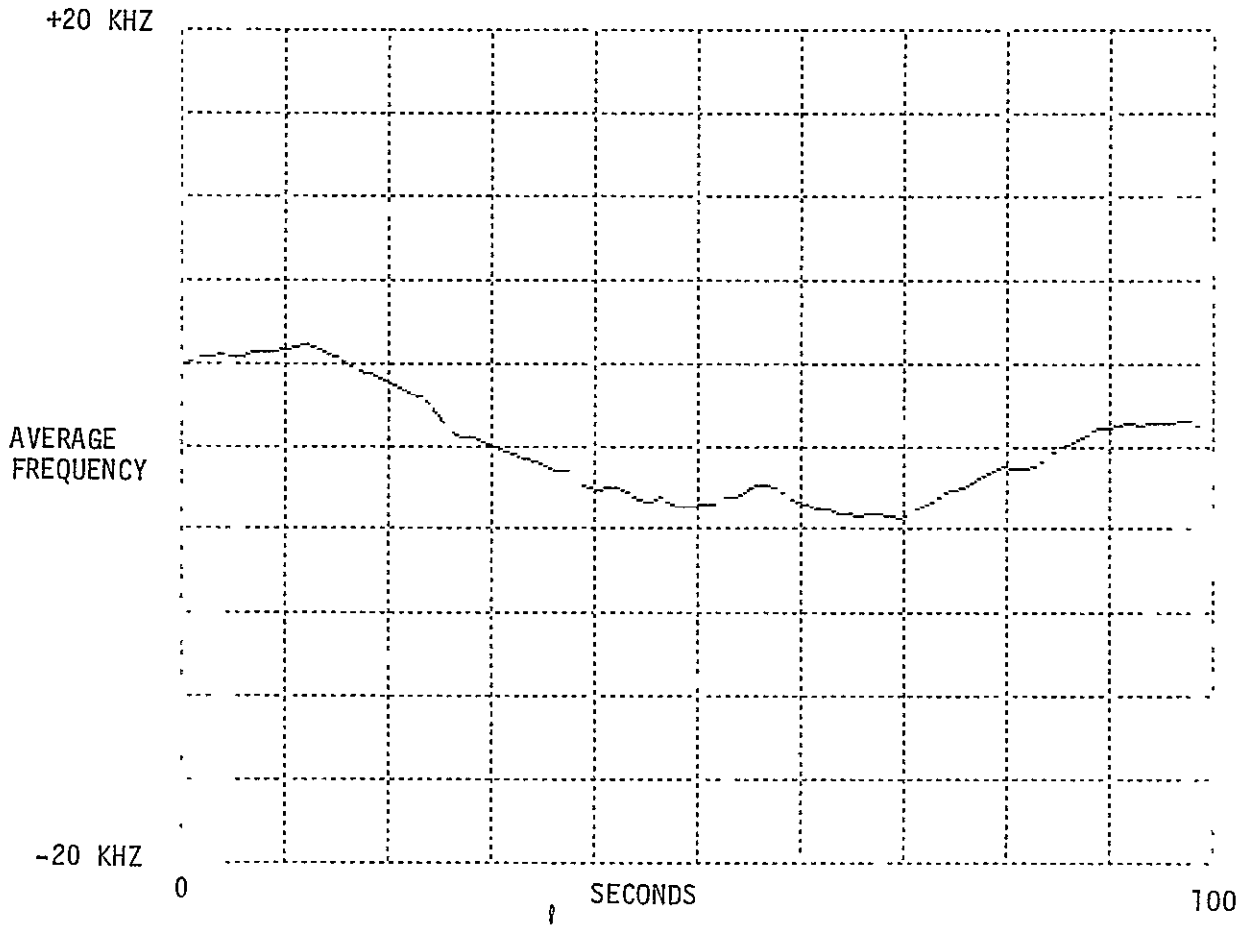


FIGURE C3; MEASUREMENT OF FREQUENCY DRIFT
1 SECOND/MEASUREMENT
100 HZ RESOLUTION
AVERAGE FREQUENCY = 15.000 GHZ

In comparison, the drift of the local oscillator is much less than that of the millimeter wave source, and is essentially negligable.

The output of the local oscillator is input to two Western Microwave 18 dB isolators operating in series. This gives a total isolation of 36 dB. These isolators absorb reflections (which could cause frequency changes) from the mixer

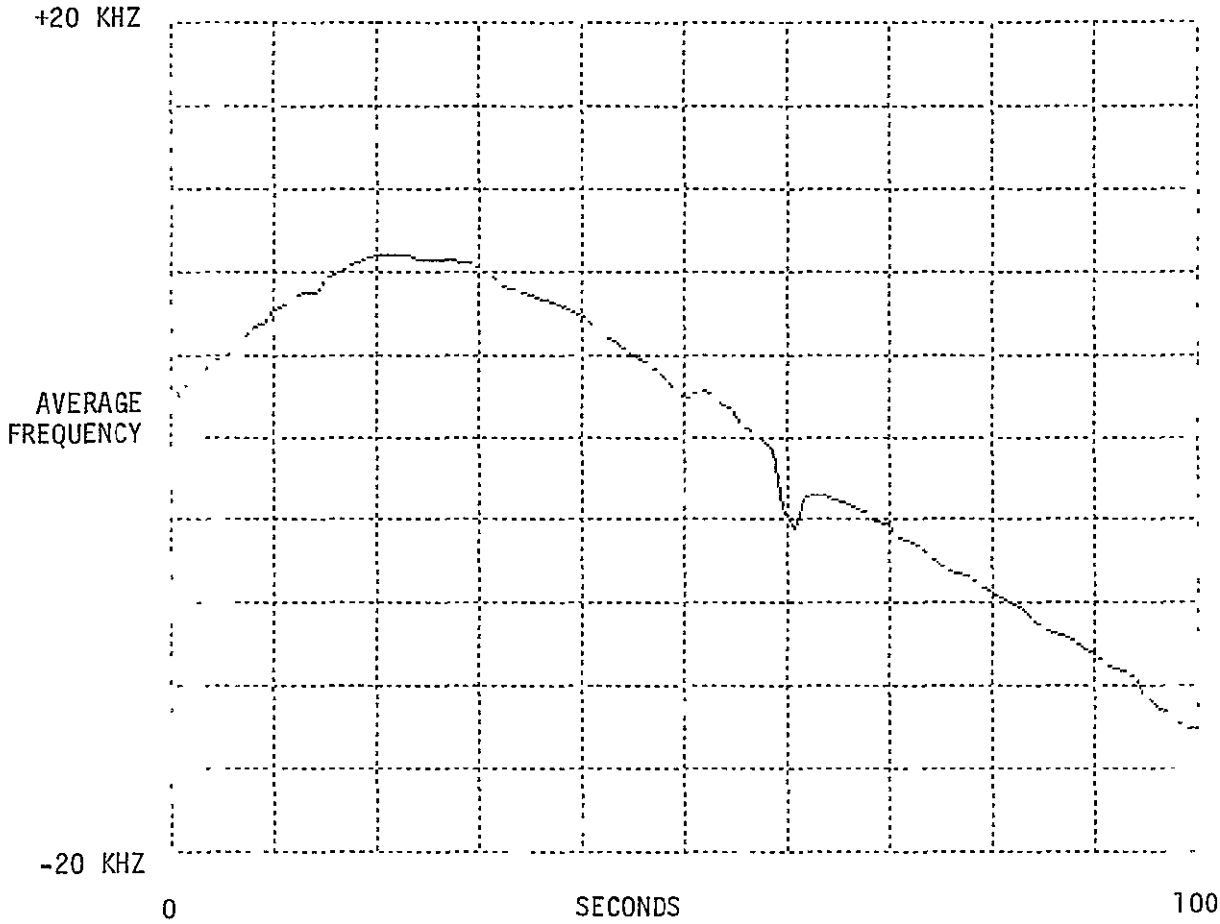


FIGURE C4; MEASUREMENT OF FREQUENCY DRIFT
1 SECOND/MEASUREMENT
100 HZ RESOLUTION
AVERAGE FREQUENCY = 15.000 GHZ

back into the oscillator. These reflections are due to impedance mismatch between the source and load of the mixer.

The local oscillator and received signal are both input to the Hughes model number 474364-1001 harmonic mixer. Down conversion is accomplished by mixing the seventh harmonic of the LO signal with the carrier frequency of the received signal. This gives theoretical IF frequency of: 7 (15 GHz) - 104.725 GHz = 275

MHz, which is the difference frequency of the mixing product. The conversion loss at the seventh harmonic is very poor, being about 21 dB. This contributes to the limited range of the UCS system. A manufacturer's data sheet is given in Appendix F.

c) IF Amplifier Strip

The IF amplifier chain was designed to provide the required input level to the demodulator and to improve the receiver sensitivity. This was best accomplished by requiring a constant input level of +16 dBm to the demodulator.

A constant input level is maintained by using a automatic gain control (AGC) amplifier. The AGC amplifier chosen is a Watkins Johnson model number 6210-320. It gives a constant power output of +7.5 dBm for an input range of -50 dBm to +5 dBm. It has a noise figure of 6.5 dB. Appendix F contains a manufactures data sheet of the AGC amp.

An additional 8.5 dB of gain was needed to meet the demodulator requirements. This was accomplished by inserting an amplifier stage after the output of the AGC amp. This is at point C as shown in Figure C5. The stage consists of a WJ-A59 IF amplifier with a 3 dB attenuator pad on the input. The WJ-A59 has a gain of 11.5 dB with a noise figure of 5.5 dB. For a +16 dBm output, the drive power requirement is: Pd = 16-11.5 = 4.5 dBm. The 3 dB attenuator provides the proper interfacing between the AGC output and IF amp input requirement.

The theoretical minimum detectable signal at the input of the AGC amp (point B in Figure C5) is given by: $S = K\ T_0\ BF\ (S/N)$ where K is Boltzmans constant, T_0 is the ambient temperature, B = bandwidth, F = noise factor, and (S/N) = signal/noise ratio. For design purposes we choose F = 2, B = 130 X 10^6 Hz, and

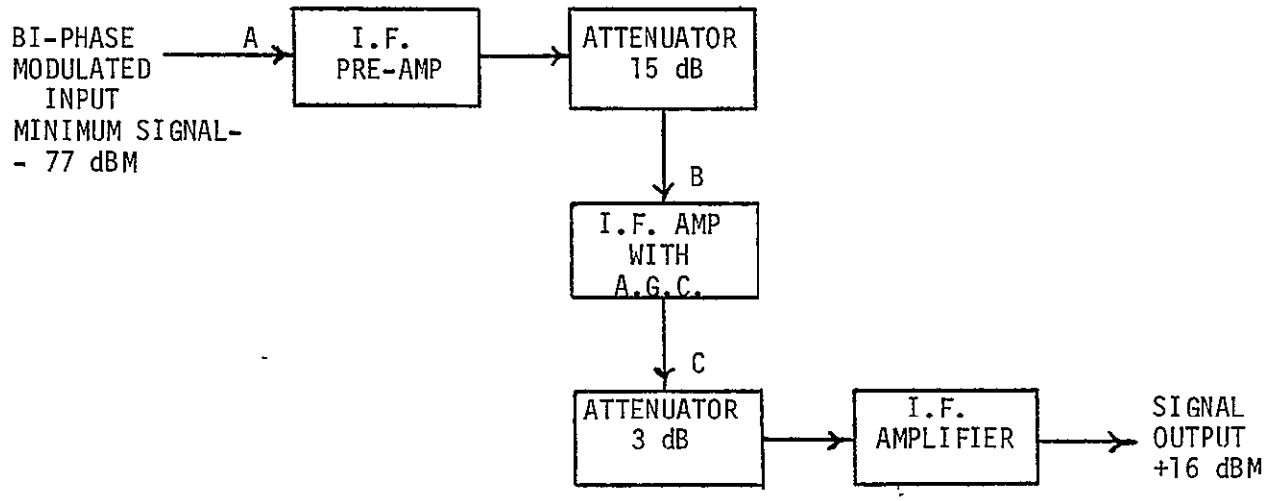


FIGURE C5; I.F. AMPLIFIER STRIP

S/N = 10. This gives S = -79 dBm. Clearly this value is too low for the AGC amp to give a constant level output and therefore our receiver sensitivity will not be improved. This result implies that an IF preamp stage is needed.

The IF preamp stage is shown in figure C5 at point A. It consists of a WJ 6200-353 cascaded amplifier, followed by a 15 dB attenuator. This amplifier has a gain of 42 dB and a noise figure of 3 dB. The 15 dB attenuator is used for proper interfacing.

With this stage added to the chain the theoretical noise figure is 3 dB (from $F = F_1 + \frac{(F_2-1)}{G_1} + \frac{(F_3-1)}{G_1 G_2}$), and the input level to the AGC is -50 dBm.

A complete schematic of the IF amplifier chain is shown in Drawing 4 of Appendix I.

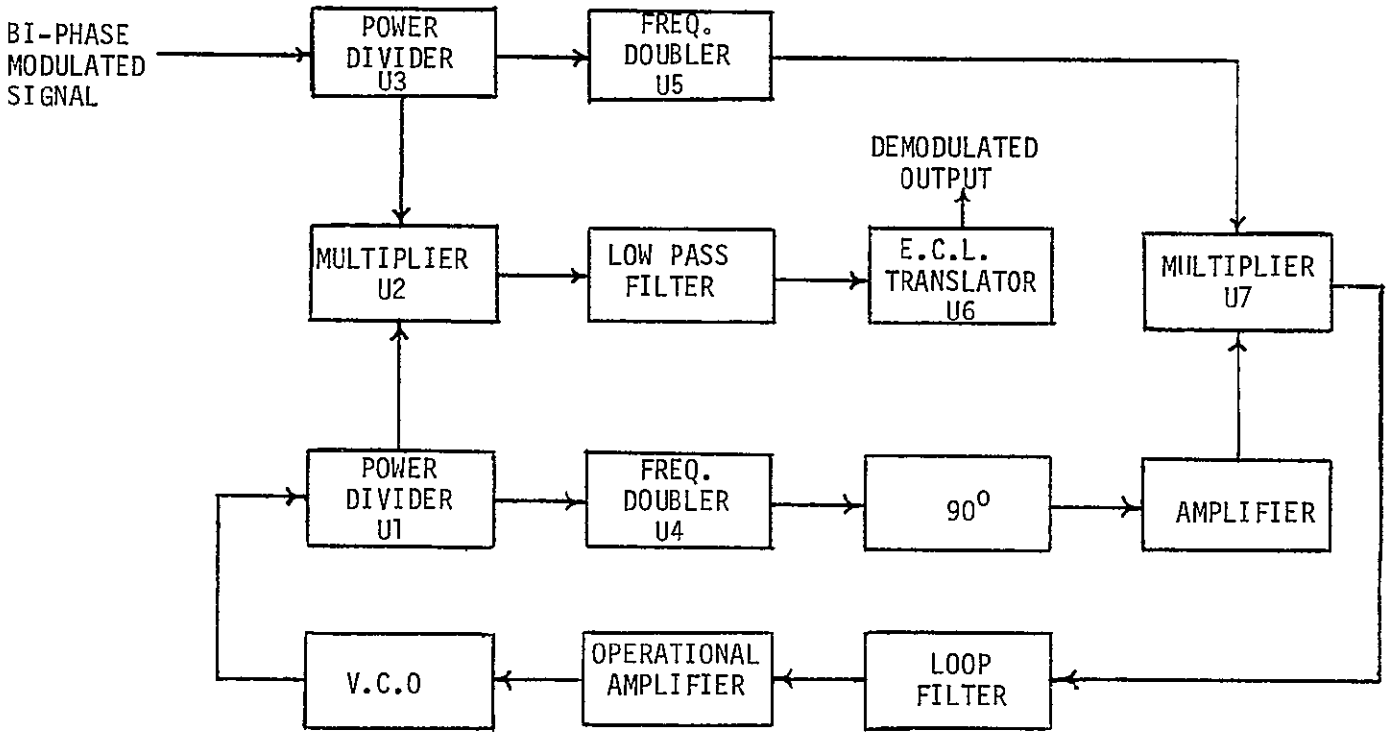


FIGURE C6; BIPHASE DEMODULATOR USING SQUARING LOOP FOR CARRIER RECOVERY

d) Bi-phase Demodulator

Figure C6 shows the bi-phase demodulator which uses a squaring loop for carrier recovery. The signal is input to a power divider (U3) from the IF amplifier chain. Here the signal is split equally between the synchronous detector and the squaring loop. In the squaring loop the frequency doubler, (U5), strips off the modulation leaving a double frequency carrier.

In order to recover the carrier, a phase locked loop locks a voltage controlled oscillator (VCO) signal to the double frequency carrier. This is accomplished by inputting the VCO signal to a power divider (U1). Here the signal is equally split between the synchronous detector and the squaring loop. In the squaring loop the frequency is doubled by the frequency multiplier (U4) and then

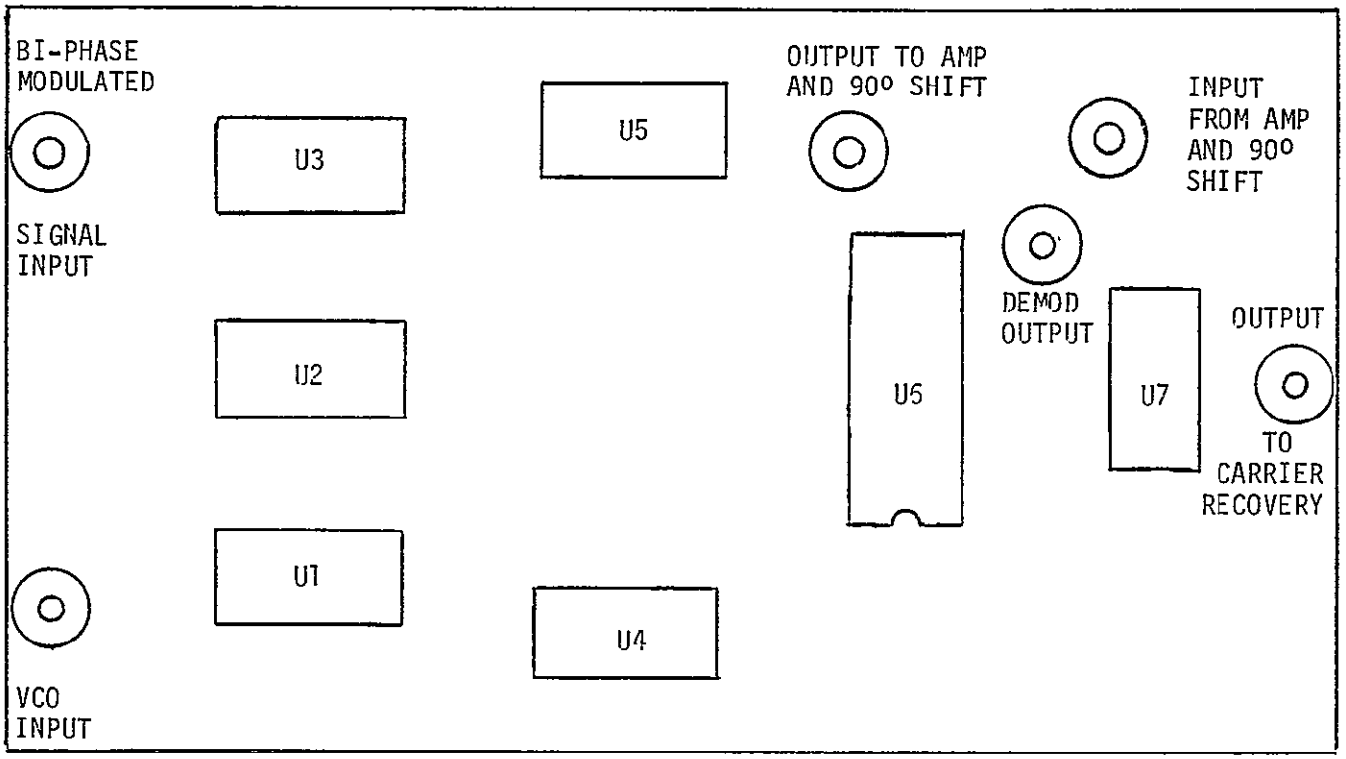


FIGURE C7; BI-PHASE DEMODULATOR BOARD LAYOUT

amplified. This signal is then compared to the input carrier in the frequency multiplier (U7) of the PLL. The output is passed through the remainder of the PLL, and used as the tuning voltage for the VCO. (This is also the error signal used in the tuning of the receiver, as described in Appendix A.) The output of the VCO is then equal to the carrier frequency and phase shifted by 90 degrees from the carrier signal. Thus it is passed through a phase shifter in the squaring loop so it can be used as the reference signal in the synchronous detector. Figure C7 shows the physical board layout for the squaring loop and synchronous detector.

In the synchronous detector the reference carrier and the received signal are mixed together in the mixer (U2). The output is lowpass filtered and translated to ECL levels to give the demodulated signal.

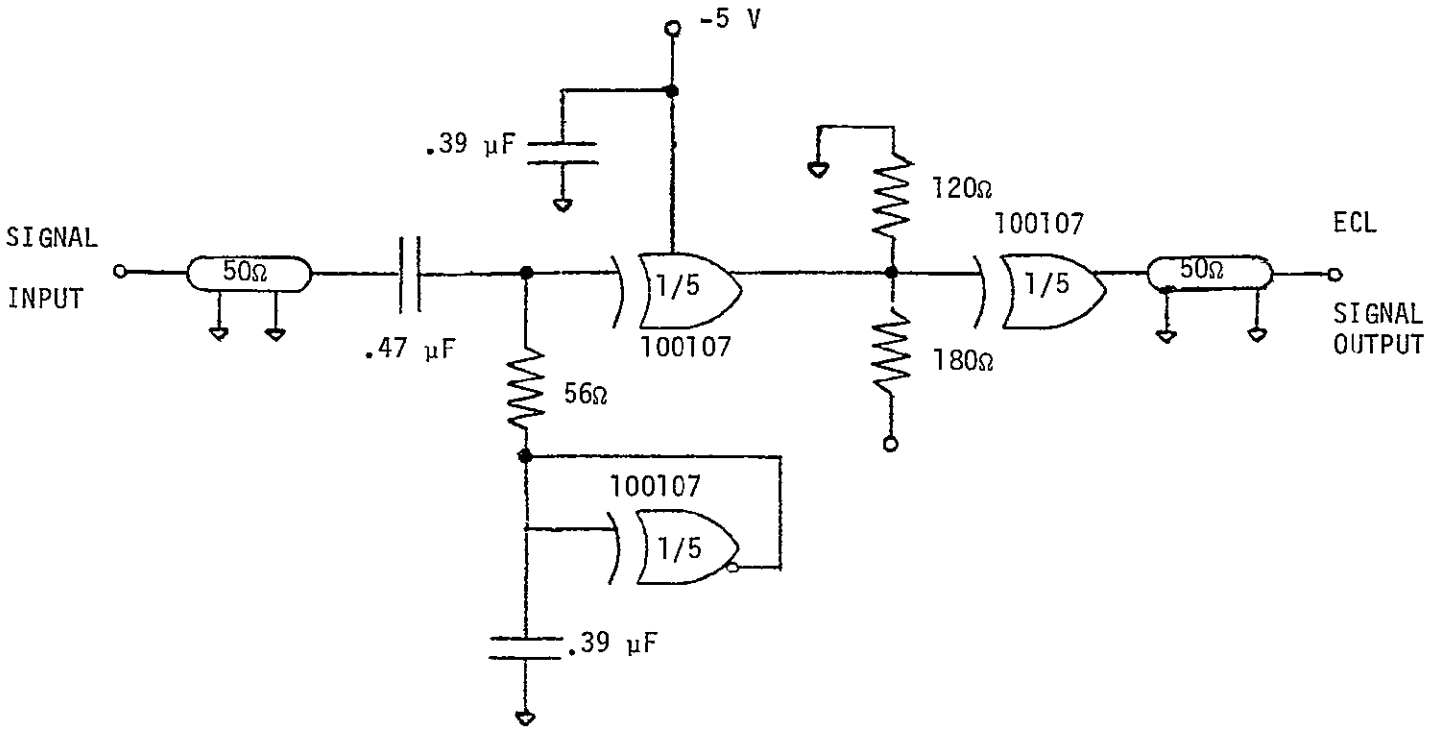


FIGURE C8; ECL TRANSLATOR CIRCUIT

The lowpass filter used in the synchronous detector is a three pole Butterworth filter. It was found to have a cut off frequency of 65 MHz. This is sufficient to provide the demodulated output to the ECL translator section. A schematic of this filter is shown in Drawing 4 of Appendix I.

The ECL translator circuit converts the demodulated bit serial stream to ECL logic levels that can be used by the D/A demultiplexer subsystem. A schematic of translator circuit is shown in Figure C8 and in Drawing 4 of Appendix I. The basis of operation is the exclusive Or gate (U6) with its input and output con-

nected together. The only voltage that satisfies both the input and output is the interal reference voltage, -1.3 volts. The input signal is then pulled down to be centered at the reference voltage. The two other gates square the signal and it is output at ECL levels.

A demodulator which uses carrier recovery has a theoretical 3 dB better noise performance than other demodulation systems. In order to take advantage of this, it was necessary to ensure that the components were operating with minimum noise. This resulted in an input power requirement to the demodulator of +16 dBm. This is a main specification used for the design of the IF amplifier strip.

Since the received signal bits can have a phase of either 0 or 180 degrees relative to the carrier, the demodulated output is either the desired signal or the negative of the desired signal. This ambiquity is resolved by transmission of a reference signal used by the data invert circuit in the DDACS.

The phase locked loop used in the carrier recovery process was designed to track the drift in the millimeter wave oscillator. In order to design the PLL we need to determine the transfer characteristics required for each of the components.

According to linear control theory we can model the phase locked loop as that shown in figure C9. By measuring the transfer function of the chosen VCO and phase detector we can determine the design of the other components. We will also be able to determine the natural frequency, lock in frequency and loop gain.

The transfer function of the Phase detector is:

$$e_d = K_d \sin(\theta_1-\theta_2) \approx K_d(\theta_1-\theta_2) \text{ for } (\theta_1-\theta_2) < .74 \text{ radians}$$

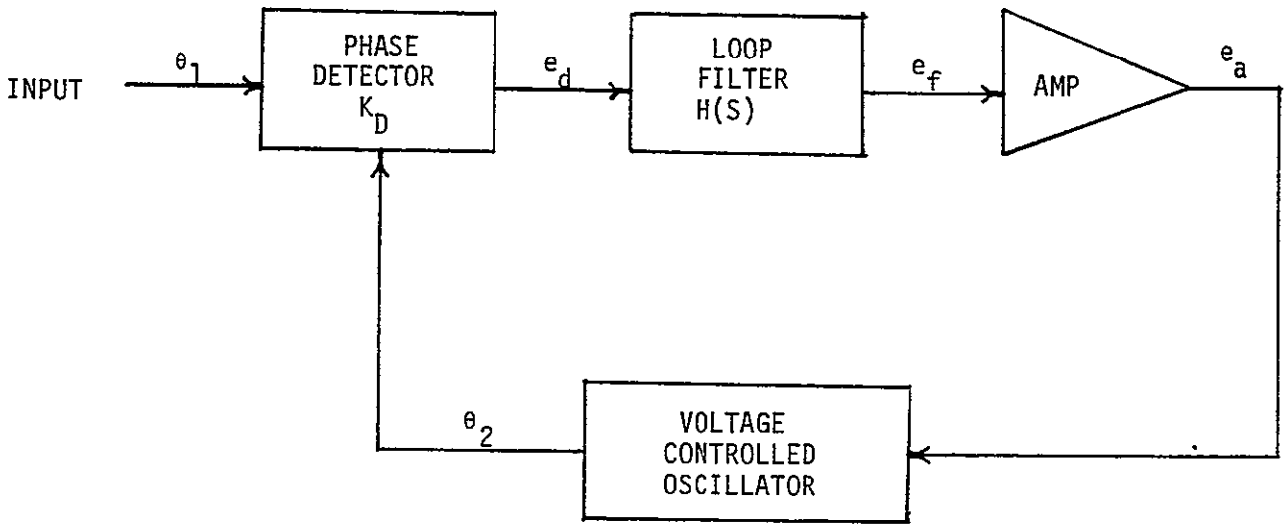


FIGURE C9; BASIC PHASE LOCKED LOOP

The loop filter chosen is a first order LPF. Its' transfer function is given by:

$$e_f = \frac{1}{2+SS_0} e_d = \frac{K_d(\Theta_1-\Theta_2)}{2+SS_0} \text{ where } S_0 = RC$$

This constitutes a filter like that shown in figure C10.

The transfer function of the loop amplifier is given by:

$$e_a = Ae_f = \frac{AK_d(\Theta_1-\Theta_2)}{2+SS_0}$$

The VCO transfer function is:

$$\frac{d\Theta_2}{dt} = K_0 e_a \rightarrow \frac{K_0 e_a}{S} = \frac{AK_d K_0(\Theta_1-\Theta_2)}{S(2+SS_0)} = \Theta_2$$

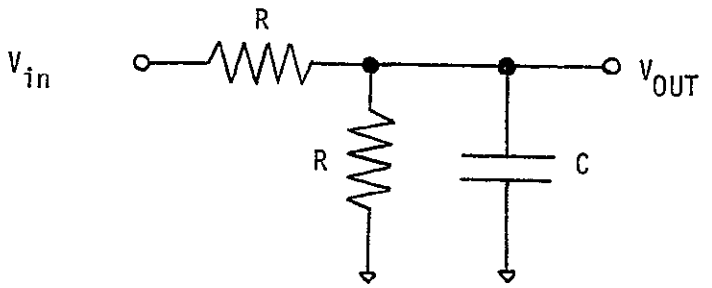


FIGURE C10; FIRST ORDER LOW PASS FILTER

Combining these relations we obtain a transfer function which relates phase error to input signal:

$$1) \quad \frac{(\Theta_1-\Theta_2)}{\Theta_1} = \frac{S(2+SS_0)}{S(2+SS_0)+AK_0K_d}$$

Further, the transfer function relating VCO phase to signal phase is:

$$\frac{\Theta_2}{\Theta_1} = \frac{AK_0K_d}{S(2+SS_0)+AK_0K_d}$$

From this we can find the magnitude of the response in the frequency domain as:

$$2) \quad \left|\frac{\Theta_2(\omega)}{\Theta_1(\omega)}\right| = \frac{1}{(1+(\omega/C)^2\Theta_t^2(4-2Y) + (\omega/C)^4\Theta_t^4Y^2)^{1/2}}$$

where $\Theta_t = \frac{C}{AK_0K_d}$ = approximate phase error for step change in frequency of $C/2\pi$ and $Y = AK_0K_dS_0$.

Using relations 1 and 2 we can determine steady state angle error, peak phase over shoot, frequency response, and cutoff frequency, all as functions of the parameters A, K_0, K_d, and S_0.

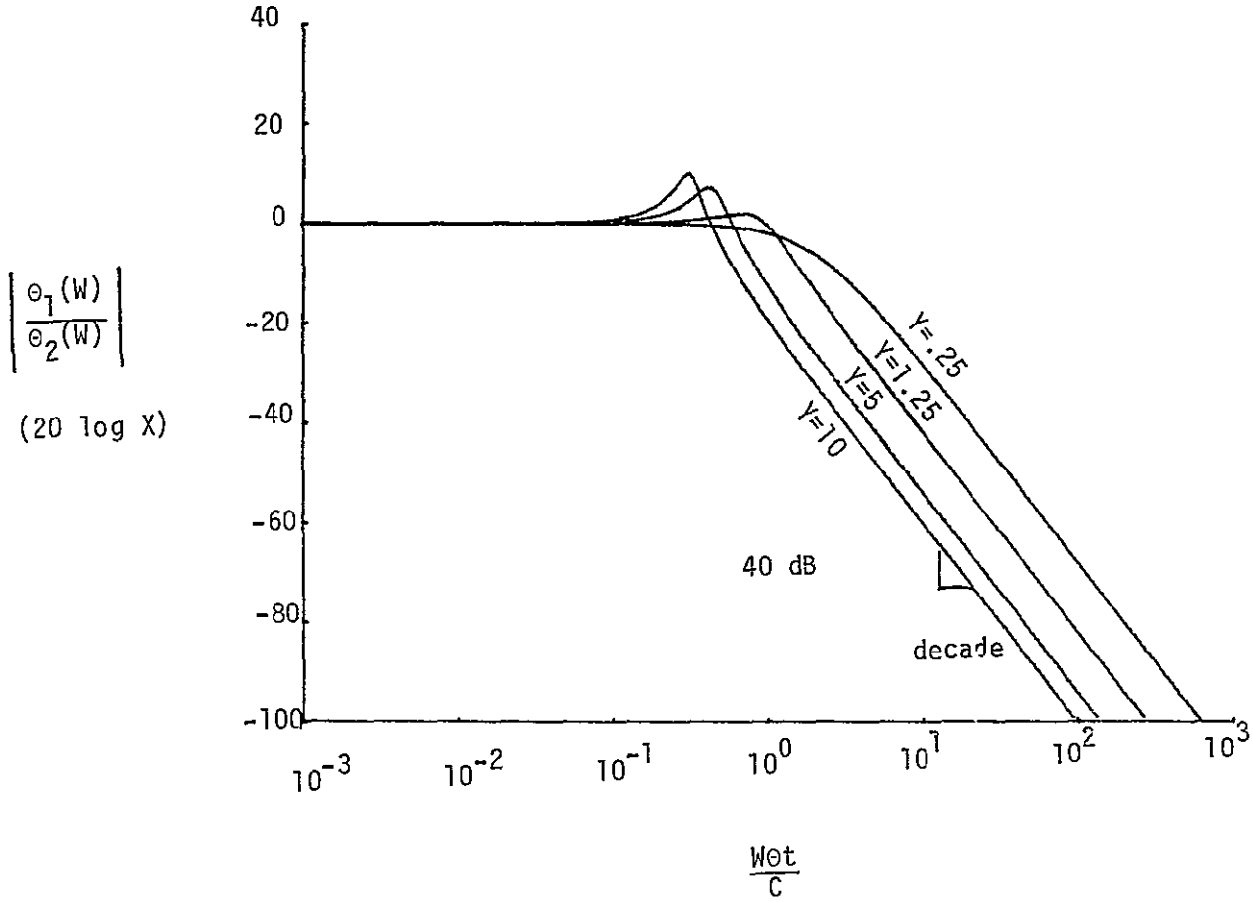


FIGURE C11; PLOT OF MAGNITUDE OF PLL TRANSFER FUNCTION FOR DIFFERENT Y VALUES

These relations were found to have several implications for our demodulator system. From equation 1 it was found that the recovered carrier will be out of phase from the actual carrier by C/AK_0K_d radians. (For a frequency drift of $C/2\pi$ Hz.) The loop gain can be tailored for acceptable error performance and a peak overshoot of <.5. Figure C11 shows a graph of equation 2 which is low pass in nature. The implication is that the PLL will track slowly varying frequency changes in the signal, while rapidly varying changes will be attenuated. The cut off frequency was found to be AK_0K_d/S_0.

Measurements of frequency drift found slow frequency deviation of ±1 MHz as shown in figures B3 and B4. Using this information the VCO we chose is a Texscan VT0200 oscillator. This gives a fast tunable voltage over 200-400 MHz. The output is isolated stabilized by using an attenuator followed by an amplifier on the output. The mixer chosen is a mini circuits SRA-1. A plot of frequency versus tuning voltage was made for the VCO and thus K_0 was found.

K_0 is given by:

$$K_0 = \frac{\Delta f}{\Delta V}$$

Also by measuring the input phase difference versus output voltage of the phase detector we can determine K_d.

Kd is given by:

$$K_d = \frac{\Delta V}{\Delta \emptyset}$$

The following parameters were chosen.

loop bandwidth = 6.5 MHz

This will give the recovered carrier 10 dB better S/N ratio than the data will have, to ensure quality demodulation.

carrier frequency = 273 MHz

f offset = ± 1 MHz

Transient error angle (overshoot) = 30%

Solving the derived relations for a S_0 and Θ_t we obtained:

$A = 10$

$\Theta_t \approx \pi/18$

$S_0 = .015$ μsec

For an $R = 50\Omega$ we found $C = 300$ pF

From these parameters the circuit shown in Drawing 4 Appendix H was realized. The extra components are for added frequency tracking, and biasing for the tuning meter.

The following parameters were measured using the demodulator circuit.

f center = 273.38 MHz

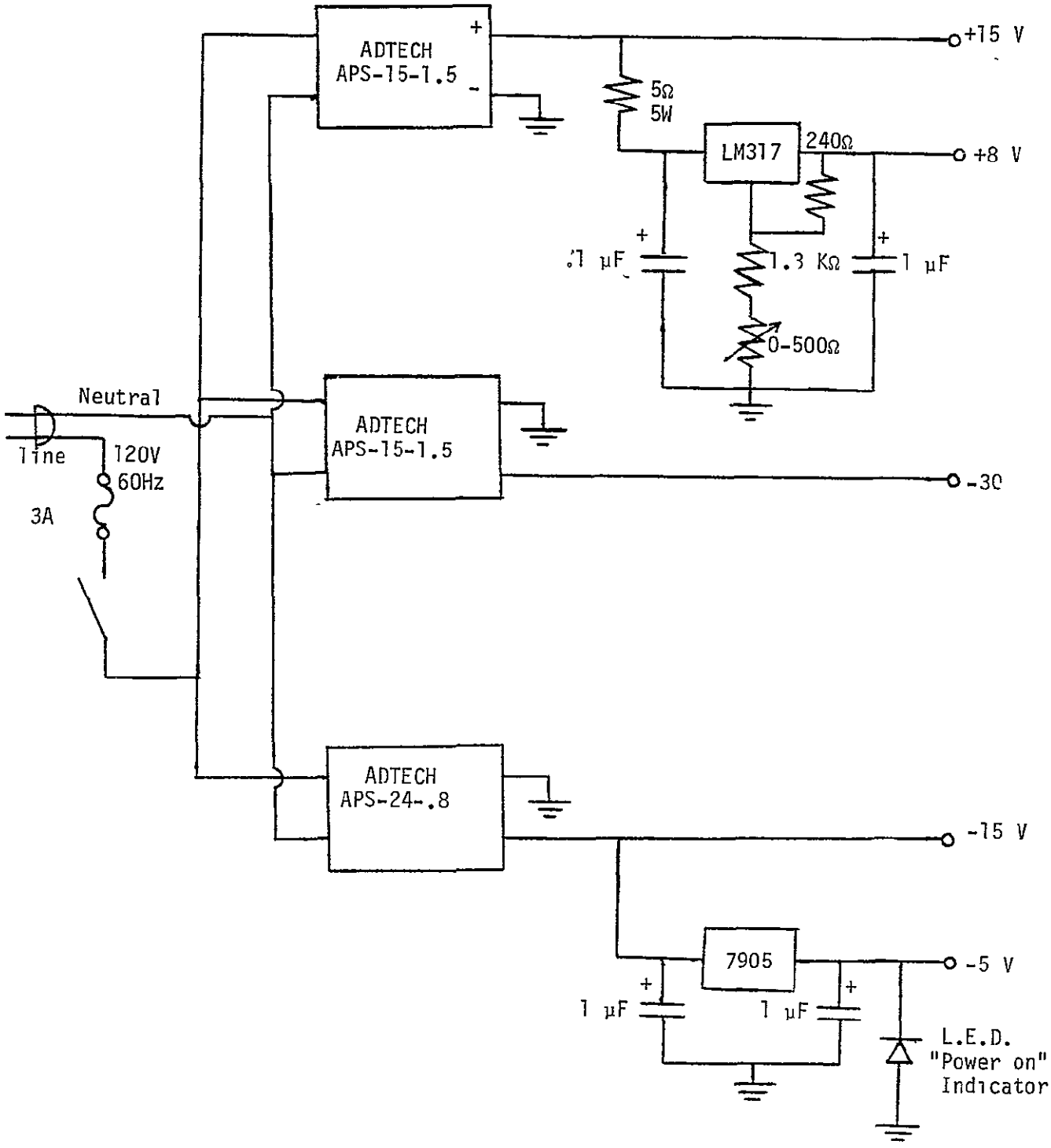
capture range 272.67 - 277.01 MHz

Locking range 270.50 - 278.8 MHz

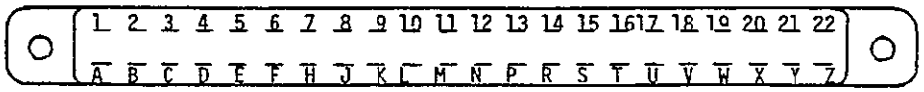
It was found that the demodulator could track frequency drift over an extended period. However coarse tuning was still periodically needed.

e) Power Supply

The power supply circuit for the receiver is shown schematically in figure C12. The power requirement for the local oscillator is +8 volts at 800 mA. The IF amplifier chain requires +15 volts at 432 mA and -15 volts at 15 mA. The voltage controlled oscillator for the bi-phase demodulator requires -30 volts at 300 mA. The remainder of the demodulator circuit has power requirements of +15 volts at 200 mA, -15 volts at 40 mA, and -5 volts at 150 mA. Commercial supplies were used for the +15, -30, and -15 volt requirements. Additional regulator circuits were used to supply the +8 and -5 volts from the commercial supplies. Figure C13 shows the connections to the receivers voltage regulator board. Figure C14 shows the terminal block voltages for the receiver power distribution.



C12; POWER SUPPLY SCHEMATIC FOR UCS RECEIVER



Pin	Connection
1	N.C.
2	N.C.
3	N.C.
4	N.C.
5	N.C.
6	GND
7	N.C.
8	+8 V OUTPUT
9	N.C.
10	+15 V INPUT
11	N.C.
12	N.C.
13	FINE TUNE INPUT (+8V)
14	N.C.
15	N.C.
16	N.C.
17	-5 V OUTPUT
18	N.C.
19	-15 V INPUT
20	N.C.
21	GND
22	N.C.

Pin	Connection
A	N.C.
B	N.C.
C	N.C.
D	N.C.
E	N.C.
F	GND
H	N.C.
J	+8 V OUTPUT
K	N.C.
L	+15 V INPUT
M	N.C.
N	N.C.
P	FINE TUNE INPUT (+8V)
R	N.C.
S	N.C.
T	N.C.
U	-5 V OUTPUT
V	N.C.
W	-15 V INPUT
X	N.C.
Y	GND
Z	N.C.

FIGURE C13; EDGE CARD CONNECTIONS ON VOLTAGE REGULATOR BOARD FOR UCS RECEIVER

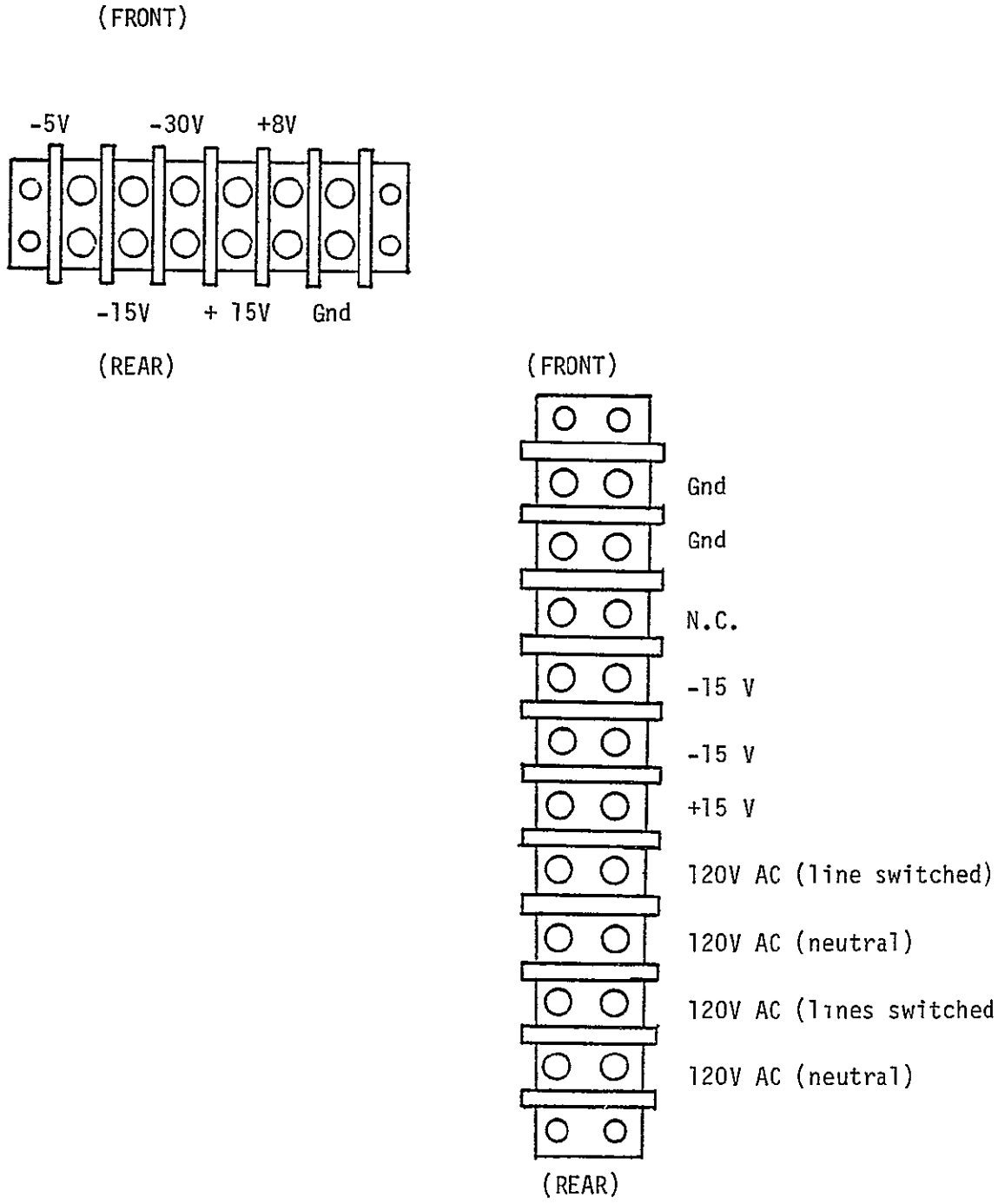


FIGURE C14; TERMINAL BLOCK VOLTAGES FOR UCS RECEIVER

APPENDIX D

DETAILED DESCRIPTION OF A/D CONVERTER AND MULTIPLEXER SUBSYSTEM

A block diagram of the ADCMS is shown in Figure D1. It shows the ADCMS composed of four major functional blocks; two A/D converters, a multiplexer and a power supply. This section describes each of these functional blocks in more detail, including operational details, schematics, and layout drawings.

a) A/D Converters

The A/D converters that were used are the TRW TDC1007PCB, which are capable of digitizing to 8 bits at up to 30 megasamples per second. The TDC1007PCB is a circuit board which is based on the TRW TDC1007J, a monolithic, LSI A/D converter. The circuit board also contains an input buffer amplifier, offset and gain adjustments, and voltage regulators. Appendix G contains the manufacturer's data sheets on the TDC1007PCB and TDC1007J converters.

One modification was made to the TDC1007PCB to allow a wider range of input offset adjustment. Resistor R4 (see pages A9 and A10 of Appendix G), of value 4.2KΩ was replaced with a 2050Ω, 1%, 0.1 Watt resistor.

In the ADCMS, the A/D converters sample at a 10 megasample per second rate, which is controlled by a CONVERT signal which originates on the multiplexer board. Only the six most significant bits (D1 - D6) are used by the multiplexer; bits D7 and D8 are ignored. Figure D2 shows the multiplexer edge card connections for the A/D converters.

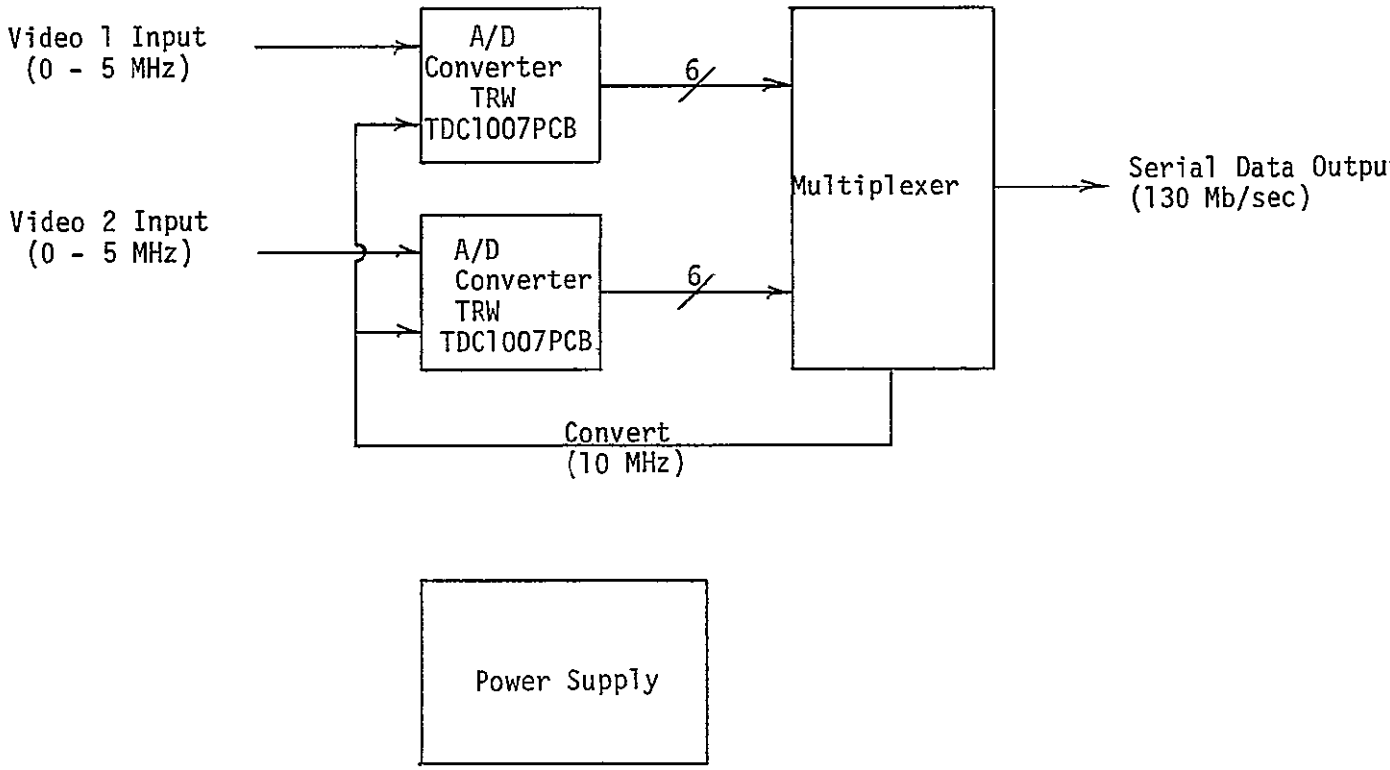
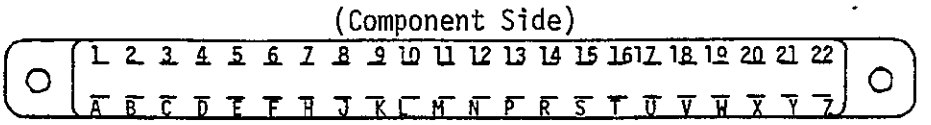


Figure D1. Block Diagram of A/D Converter and Multiplexer Subsystem (ADCMS)

b) Multiplexer Board

The multiplexer board multiplexes the A/D outputs into a serial stream, and performs several buffering and timing operations essential to operation of the ADCMS. All components are mounted on a single multilayer printed circuit board. Drawing 1 (Appendix H) is a schematic of the board, while Figure D3 shows its physical layout. The multiplexer uses emitter-coupled logic (ECL) in order to obtain the digital speeds required. All ECL parts used are Fairchild 10K and 100K series.



Pin	Connection	Pin	Connection
1	AGND	A	N.C.
2	AGND	B	N.C.
3	AGND	C	N.C.
4	AGND	D	N.C.
5	AGND	E	-15V
6	AGND	F	N.C. (REF IN)
7	AGND	H	+15V
8	AGND	J	N.C.
9	AGND	K	ANALOG INPUT
10	N.C.	L	N.C.
11	DGND	M	+5V
12	DGND	N	CONVERT
13	DGND	P	N.C. (D8)
14	DGND	R	+5V (NMINV)
15	DGND	S	D1 (MSB)
16	DGND	T	D2
17	DGND	U	D3
18	DGND	V	D4
19	DGND	W	+5V (NLINV)
20	DGND	X	D5
21	DGND	Y	D6 (LSB)
22	DGND	Z	N.C. (D7)

Figure D2. Edge Card Connections for A/D Converters

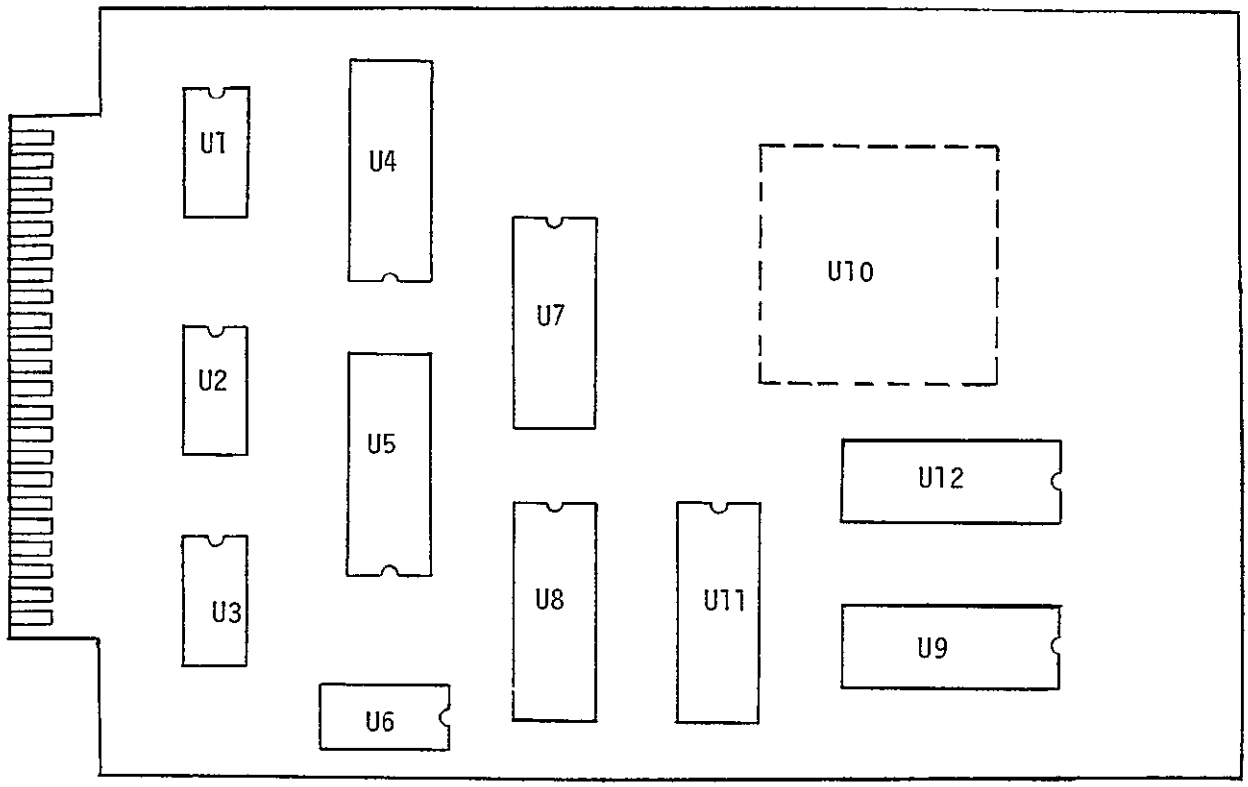


Figure D3. Physical Layout of Multiplexer Board

The outputs of the A/D converters are TTL level signals, which are converted to ECL on the multiplexer board by three 10124 TTL-ECL converters, U1-U3. Once converted to ECL, the data are latched by two 100151 hex flip-flops, devices U4 and U5. These hold the data constant at the multiplexer chip input during each sample period, so that all twelve data lines can be multiplexed. U7 is a 100164 16 input multiplexer, which multiplexes the 12 data lines and one synchronization line into a serial bit stream at Z output. The digital data from A/D converter #1 appears at pins I_{11} (MSB) through I_6 (LSB) of U7, and the digital data from A/D converter #2 appears at pins I_5 (MSB) through pins I_0 (LSB). The synchronization bit was chosen to be a constant logic zero at pin I_{12}.

The clock for the multiplexer board is provided by a Vectron CO-233ME-B crystal clock oscillator. The oscillator frequency is 130 MHz and its output is ECL compatible.

The 100136 four bit counter (U11) provides all of the timing and synchronization signals for operation of the multiplexer and A/D converters. The counter is configured to be preset to a digital "12" (i.e., $Q_3Q_2Q_1Q_0$ = 1100 binary) and count down to a digital "0" (0000). The digital "0" causes pin 8 of U8 to go low, which causes U11 to preset itself on the next clock pulse. Inputs $P_3P_2P_1P_0$ are configured 1100, which presets the counter to digital "12" once again, and the cycle repeats. Inputs P_3 and P_2 are held high by a diode connected to ground, inputs P_1 and P_0 are pulled low by internal pulldown resistors.

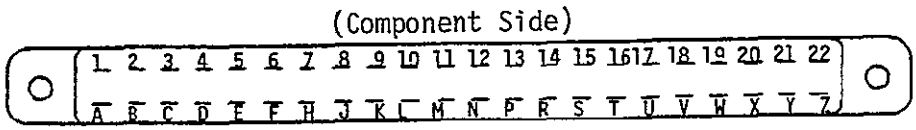
The outputs of U11 are bussed to the control inputs of U7 and perform the function of selecting the input line which appears at the Z output of U7. If the output of the counter is a digital "12" (1100), then input I_{12} of the multiplexer is presented at the multiplexer output. Similarly, a counter output of "11" selects line I_{11} and etc.

The strobe signal for U4 and U5 is generated by NOR'ing outputs $\overline{Q}_2$ and $\overline{Q}_3$ of U11. The result is a signal which is high when the counter registers a digital "12" and is low otherwise. New data is strobed into the flip-flop as pin 10 of U8 makes the low-to-high transition. During the period that the counter output is "12", the new data appears at U7's inputs, at which time the synchronization bit (I_{12}) is being output, so that glitches in the multiplexer output do not occur due to changing input data.

The CONVERT signal which clocks the A/D converters is generated by NOR'ing the Q_2 and $\overline{Q_3}$ output of U11. The result is a signal which is high when the counter output is "8", "9", "10", or "11", and low otherwise. The resulting signal, which appears at pin 5 of U8, is a pulse signal of 10 MHz rate, and 31 nsec pulse width. This signal is converted to TTL level by the 10125 ECL to TTL converter (U6). The A/D conversion cycle is triggered by the leading edge of the CONVERT signal. Ninety nanoseconds following the low-to-high transition of pin 5 of U8, the data is clocked into U4 and U5. This allows ample time for the A/D conversion to take place, for propagation times through ECL-TTL and TTL-ECL converters, and for propagation time through interconnect wiring.

The serial output of U7 is differentially encoded by the circuitry which follows. The purpose is to randomize the data, so that long strings of data of constant value do not occur. This facilitates clock recovery in the DDACS, which will be described later. The differential encoding is performed by EXCLUSIVE-OR'ing each new output of U7 with the previous output of the EXCLUSIVE-OR gate (U12). The effect is to convert strings of constant value to strings of alternating zeros and ones. Flip flops (U9) (100131) are used to clock the inputs to the EXCLUSIVE-OR and prevent glitches by ensuring that both inputs arrive at the EXCLUSIVE-OR gate simultaneously. An additional EXCLUSIVE-OR gate serves as a buffer between the board and the outside world.

The schematic does not show termination resistors or power supply bypass capacitors. All ECL traces are 70Ω microstrip, and are terminated to -2 volts with 68Ω, 1/8 watt resistors, the location of which are layout dependent. Adequate power supplying bypassing is included on the board to prevent the coupling of signals into the power supply.



Pin	Connection
1	-5V
2	-5V
3	-2V
4	-2V
5	-5V
6	-5V
7	GND
8	GND
9	GND
10	GND
11	GND
12	GND
13	GND
14	GND
15	GND
16	GND
17	+5V
18	+5V
19	-5V
20	-5V
21	-2V
22	-2V

Pin	Connection
A	GND
B	-5V
C	-5V
D	D5-2
E	D6-2 (LSB)
F	D4-2
H	D3-2
J	D1-2 (MSB)
K	D2-2
L	D6-1 (LSB)
M	D5-1
N	GND
P	GND
R	GND
S	D3-1
T	D4-1
U	D2-1
V	D1-1 (MSB)
W	CONVERT
X	GND
Y	GND
Z	GND

Figure D4. Edge Card Connections for Multiplexer Board

Figure D4 shows the multiplexer board edge card connections.

c) Power Supply

The power supply for the ADCMS is shown schematically in Figure D5. The power requirement for each A/D converter is +15 volts at 50 mA, -15 volts at 500 mA and +5 volts at 125 mA. The power supply requirement for the multiplexer board is +5 volts at 250 mA, -5 volts at 1300 mA and -2 volts at 600 mA. Commercial supplies

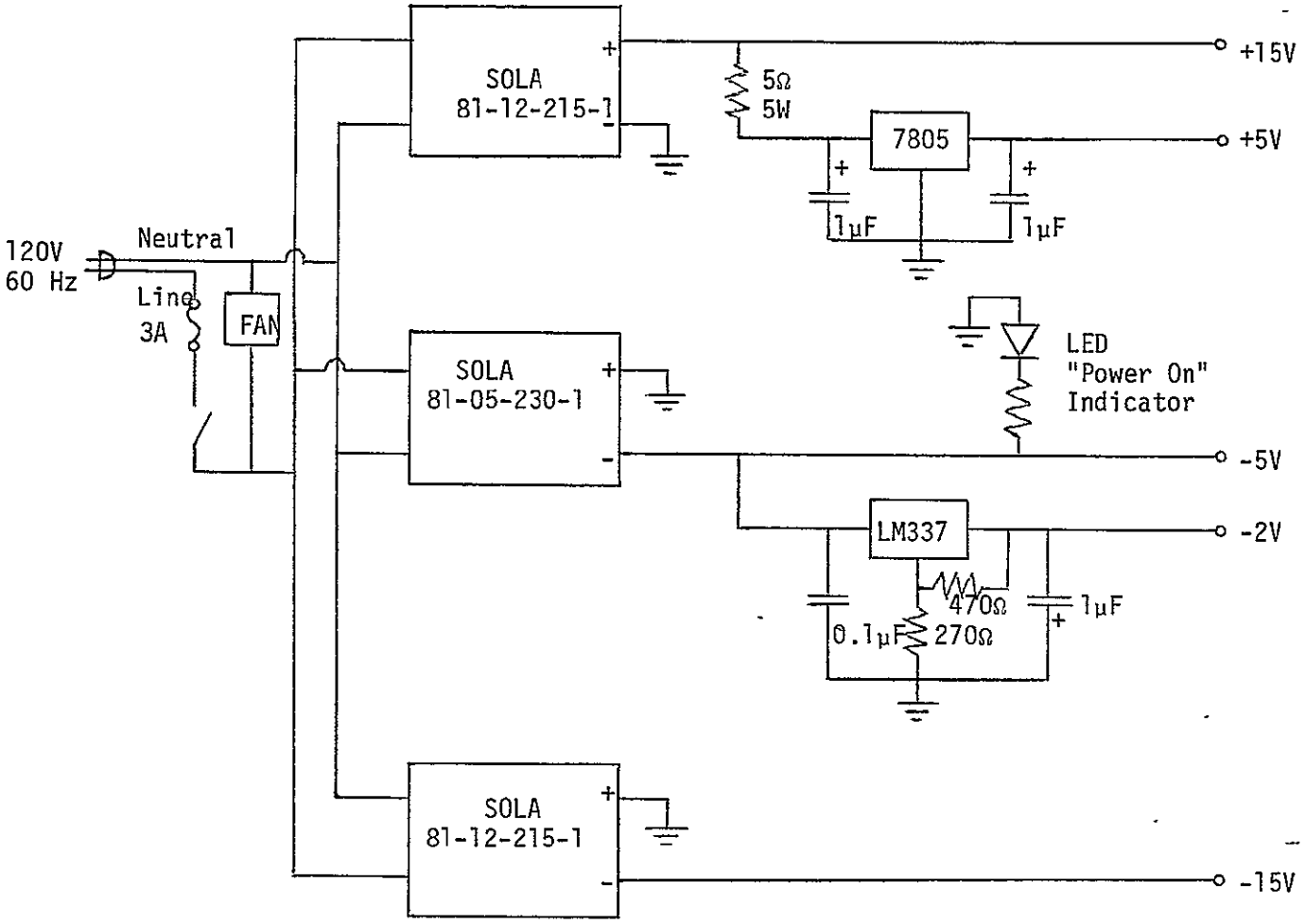


Figure D5. Power Supply Schematic for ADCMS

were used for the +15, -5 and -15 volt power, while single-chip regulators were used to provide the +5 and -2 volt supplies. Figure D6 shows the voltages at the power distribution terminal strip.

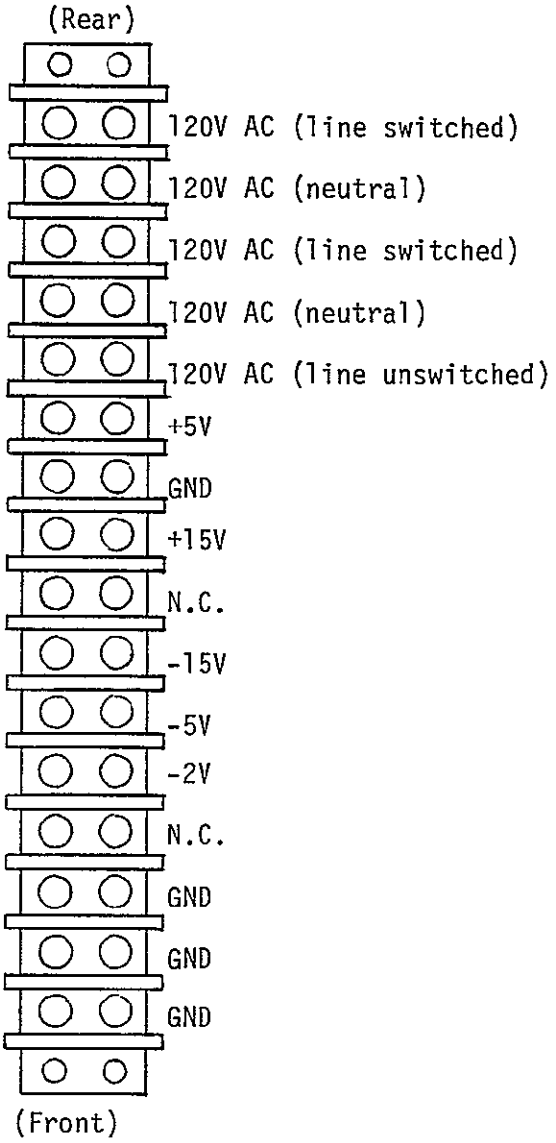


Figure D6. Terminal Block Voltages for ADCMS

APPENDIX E

DETAILED DESCRIPTION OF DEMULTIPLXER AND D/A CONVERTER SUBSYSTEM

A block diagram of the DDACS is shown in Figure E1. The four major functional blocks are: a) the clock recovery circuit, b) the demultiplexer and D/A converters, c) the synchronization circuit, and d) the power supply. The clock recovery circuit takes the input serial data stream and extracts a clock signal from it. Both data and clock are passed to the demultiplexer and D/A circuit, which differentially decodes the data stream, identifies the synchronization bit, and demultiplexes the data into two 6-bit parallel data streams at 10 Mb/second each. These are fed to two D/A converters and low pass filters which convert them to 0 - 5 MHz video signals. The automatic data invert circuit decides whether the polarity of the incoming data stream is correct, and if not, automatically inverts it. Power supplies provide the power for the DDACS. Each of the major components is described in greater detail below.

a) Clock Recovery Circuit

The clock recovery circuit, as mentioned previously, recovers a clock signal from the incoming data stream. The clock is then used for timing by later processing circuits. The clock recovery circuit looks for transitions in the incoming data. Each time a transition occurs, a pulse is created by a special logic circuit. A voltage controlled oscillator is then phase-locked to this generated pulse stream. Since the incoming data cannot have a transition for every data period, the pulse stream will have missing pulses; in other words, there will not be a pulse for every data period. Because of the differential encoding in the ADCMS however, a pulse will occur for approximately 50% of the data time slots. The bandwidth of the feedback signal of the phase-locked loop is narrow, so that

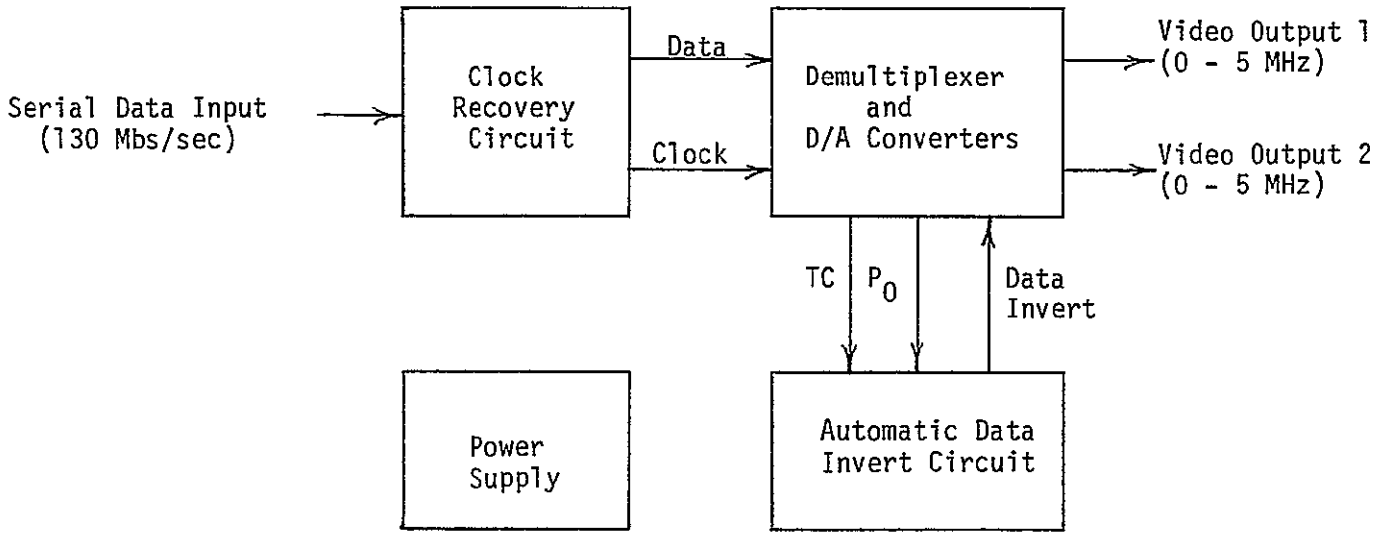
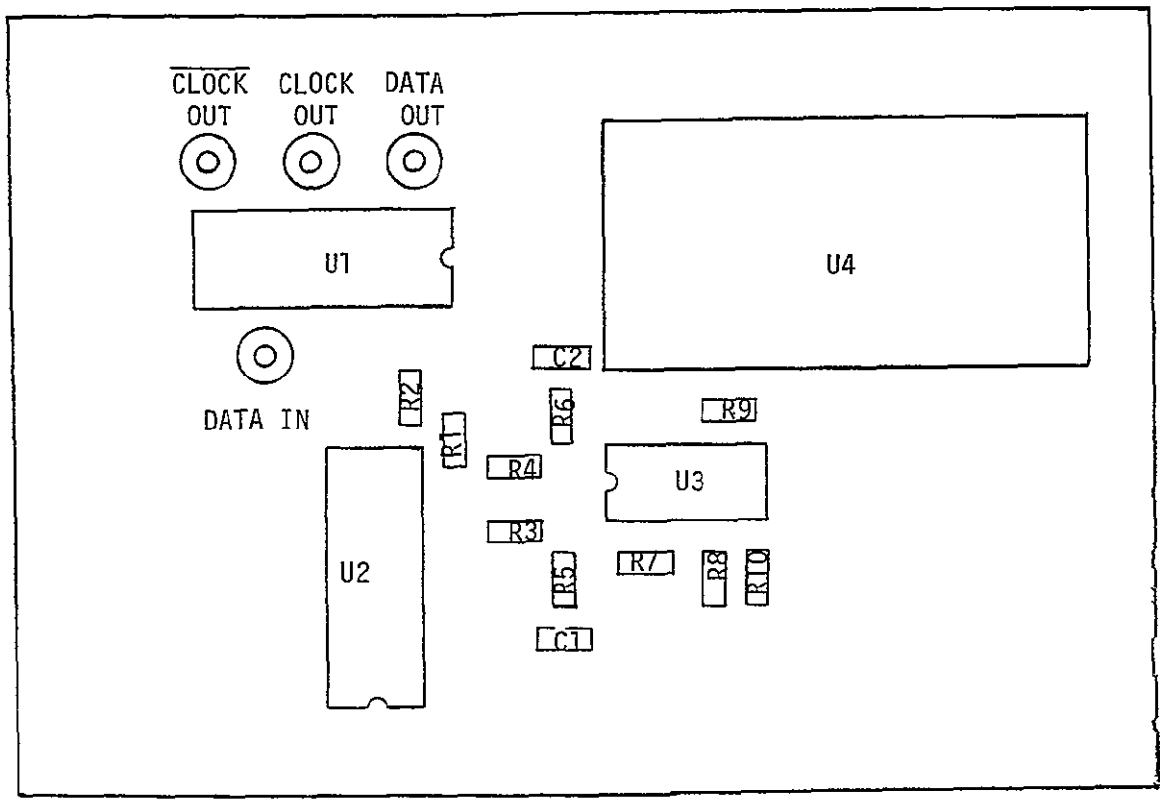


Figure E1. Block Diagram of Demultiplexer and D/A Converter Subsystem (DDACS)

the phase-locked loop will drift through those periods when pulses are missing and not change significantly in frequency.

Drawing 2 in Appendix H shows a schematic diagram of the clock recovery circuit. The input, a 130 Mb/sec ECL signal, is buffered by an EXCLUSIVE-OR gate. The output of this gate, pin 13 of U1, goes to the inputs of another EXCLUSIVE-OR gate by two different paths. Pin 17 of U2 receives the signal by a direct path, while pin 16 of U2 receives the signal delayed by 3.6 nsec. The delay is implemented by running the signal through three EXCLUSIVE-OR gates in series. The output of this EXCLUSIVE-OR gate is low whenever the data is unchanging, and a 3.6 nsec high pulse whenever the data changes logic levels. The width of the pulse, 3.6 nsec, is approximately one-half the period of a 130 MHz clock signal. The pulse output is compared to the output of a voltage-controlled clock oscillator (Vectron 275-4909, which has an ECL compatible output) by an EXCLUSIVE-OR gate. The gate output (pin 13 of U2) is high whenever the two inputs

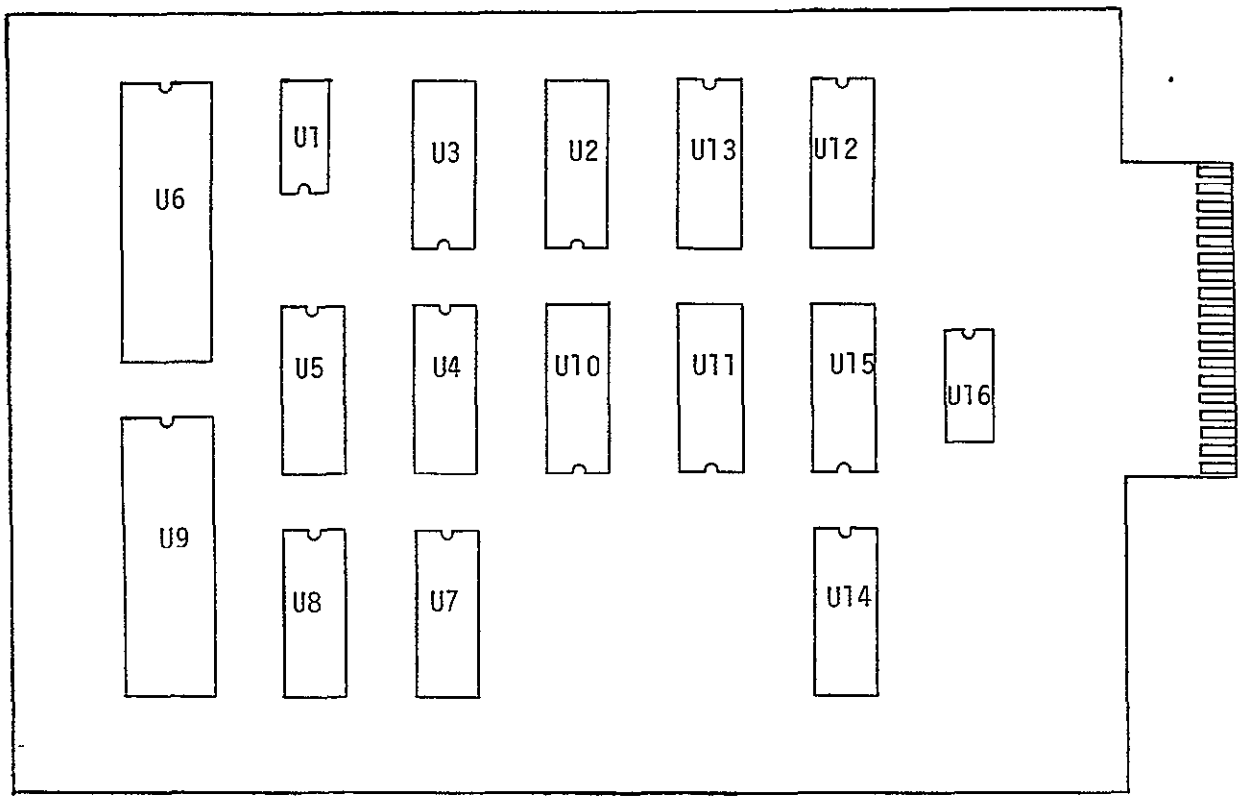


(Viewed from Component Side)

Figure E2. Physical Layout of Clock Recovery Circuit

have different logic levels, and low whenever the two signals have the same logic level. The effect is similar to multiplying two bipolar signals. Both the inverted and noninverted outputs are low-pass filtered to give a loop error signal. A differential amplifier with gain of 10 amplifies the signal to feed back as the VCO tuning voltage. The feedback loop causes the VCO to lock 90° out of phase with the pulse signal, in order to drive the loop error signal to zero.

The circuit outputs are the original ECL data stream and the inverted and noninverted output of the VCO. All outputs are buffered by EXCLUSIVE-OR gates. Figure E2 shows component locations on the clock recovery board.



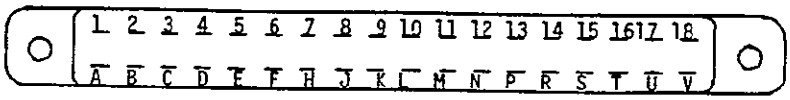
(Viewed from Component Side)

Figure E3. Physical Layout of Demultiplexer and D/A Converter Board

b) Demultiplexer and D/A Converter Board

This board provides the DDACS with the functions of differential decoding, demultiplexing, synchronization, and D/A conversion. A schematic is shown in Drawing 3, Appendix B. Figure E3 shows the Physical layout of the board, and Figure E4 shows edge card connections.

The differential decoding reverses the differential encoding that is performed in the ADCMS, recovering the original (unencoded) data. The decoding is done by EXCLUSIVE-ORing a received bit with the previous bit that was received. The ouptut of the EXCLUSIVE-OR (pin 11 of U3) is the decoded data. Flip-flops are used to sequence the data into the EXCLUSIVE-OR inputs so that glitches do not occur due to timing offsets.



(Component Side)

Pin	Connection
1	GND
2	GND
3	GND
4	GND
5	GND
6	GND
7	GND
8	+5V
9	Data Invert Input
10	P_0 Output
11	TC Output
12	+5V
13	GND
14	GND
15	GND
16	GND
17	Video 1 Output
18	Video 2 Output

Pin	Connection
A	-5V
B	-5V
C	-5V
D	-5V
E	-2V
F	-2V
H	-2V
J	GND
K	GND
L	GND
M	GND
N	GND
P	-2V
R	-2V
S	-2V
T	Analog GND
U	Analog GND
V	Analog GND

Figure E4. Edge Card Connections for Demultiplexer and D/A Converter Board

The demultiplexing process begins in the 100141 8-bit shift registers U4 and U7. Each data period, the current data bit is clocked into U4, and the previous data bits are shifted by one position. Every thirteenth clock cycle, twelve bits of data are strobed into a pair of 100151 hex flib-flobs, U5 and U8, which serve as buffers between the shift registers and the D/A converters. At a later time, the data is strobed from the hex flip-flops into the D/A converters.

The strobe signals for the hex flip-flops come from U10, a 100136 counter. In the normal case, when the data is already synchronized (the synchronization process will be described later), the counter counts up from "0" to "12" ($Q_3Q_2Q_1Q_0$ is 0000 to 1100). When the counter reaches "12", pin 8 of U11 goes low, which pulls control pins S_1, and S_2 of the counter low, causing the counter to reset to zero at the next clock pulse. The counter then resumes counting upward until it once again reaches "12" and resets.

The strobe for U5 and U8 is given by pin 9 of U11. This signal is high when the counter is at "12" and low otherwise. Data is strobed into U5 and U8 at the low-to-high-transition of this signal.

The strobe for the D/A converters is the Q_3 output of counter U10. This signal is high when the counter is at "8", "9", "10", "11", and "12", and is low otherwise. This provides a clock signal of approximately 38 nsec pulse width for the D/A converters (a clock of at least 15 nsec width is required). The data is clocked into the converters at the low-to-high transition of the clock signal.

At the same time that twelve bits of data are being strobed into U5 and U8, a thirteenth bit is strobed into U2, a 100131 flip-flop, at pin 3. When the circuit is synchronized, this bit will be the synchronization bit, i.e., a low. If,

however, the circuit is not synchronized, this bit could be either a low or a high. The inverted output of the flip-flop (pin 5) is NOR'd in a 100102 (U15) with the signal at pin 11 of U11, which is a low when the output of U10 is "3" and high otherwise. The output of the NOR gate (pin 11 of U15) is a constant low if the synchronization bit is a low, and a 7.7 nsec high pulse if the synchronization bit is high (in which case the circuit is not synchronized).

The number of high pulses output by the NOR gate (pin 11 of U15) is counted by U12, a 100136 counter. Each time a pulse occurs, the count is incremented by 1 until a count of "4" is reached. At this point, Q_2 (pin 8 of U12) goes high, which forces S_0 (pin 20) high and causes the counter to hold the present count. Additional pulses are ignored by the counter.

Simultaneously, while U12 is counting the number of synchronization bits that are not low, another 100136 counter, U14, counts the number of sync bits that have elapsed. Pin 10 of U11 is the clock input to this counter, and is high when the count of U10 is "3" and low elsewhere. Counter U14 is configured to count up, so each time a pulse arrives the count is increased by one. When the count reaches "15", pin $\overline{TC}$ (pin 1 of U14) goes low, which triggers several events. First, outputs Q_2 and Q_3 (pins 8 and 11) of counter U12 are clocked into U13 (100151 flip-flops). This occurs when counter U10 reaches a count of "6" (pin 4 of U11 low). Next, the count of U12 is reset to zero, which occurs when counter U10 reaches a count of "12" (pin 8 of U11 low).

Pin 12 of U15 indicates whether the circuit is synchronized or not. It results from NOR'ing outputs Q_2 and Q_3 (pins 8 and 11) of counter U12 (after clocking through U13). If U12 has reached a count of 4 or greater non-zero sync bits, Q_2 will be high, and pin 12 of U15 will be low. If fewer than 4 non-zero

sync bits are counted, then Q_2 and Q_3 will both be low and pin 12 of U15 will be high. This circuit interprets a high signal at pin 12 of U15 to mean that the circuit is correctly synchronized and a low signal to mean that the circuit is incorrectly synchronized.

After every sixteenth synch bit, TC of U14 (pin 1) goes low. If pin 12 of U15 is low, then pin 3 of U15 goes high, raising input P_0 of U10 high. This signal enables the loop to synchronize itself, for instead of loading a count of "0" into U10 at the next opportunity, it will load a "1". All timing functions will then be advanced by one bit. In this way, the multiplexer slips one bit at a time in search of the correct synchronization.

If pin 12 of U15 is high, then the synchronizer is already assumed synchronized. In this case, counter U10 loads a count of "0" and continues to do so as long as synchronization is maintained.

The probability of losing synchronization and the mean time before synchronization loss can be calculated versus signal-to-noise ratio of the data. In any sixteen synchronization bits, the probability of losing synchronization is given by the probability of seeing >3 errors in 16 bits.

$$\text{(Prob of >3 errors in 16 bits)} = \text{(prob of 4 errors)} + \text{(prob of 5 errors)} + \ldots + \text{(prob of 16 errors)}, \quad (1)$$

where the probability of seeing s errors in 16 bits is

$$\text{(Prob s errors in 16 bits)} = {}_{16}C_s P^s (1 - P)^{16-s} \quad (2)$$

where P is the probability of a bit error, and ${}_rC_s = \frac{r!}{s!(r - s)!}$.

The probability of the loop losing synchronization in a 1.6 μsec interval (16 sets of 13 data bits) is shown in Figure E5 for various data signal-to-noise ratios. It is seen that for reasonably high signal-to-noise ratios (greater than 10 dB), the probability of synchronization loss is very small (less than 1×10^{-18}).

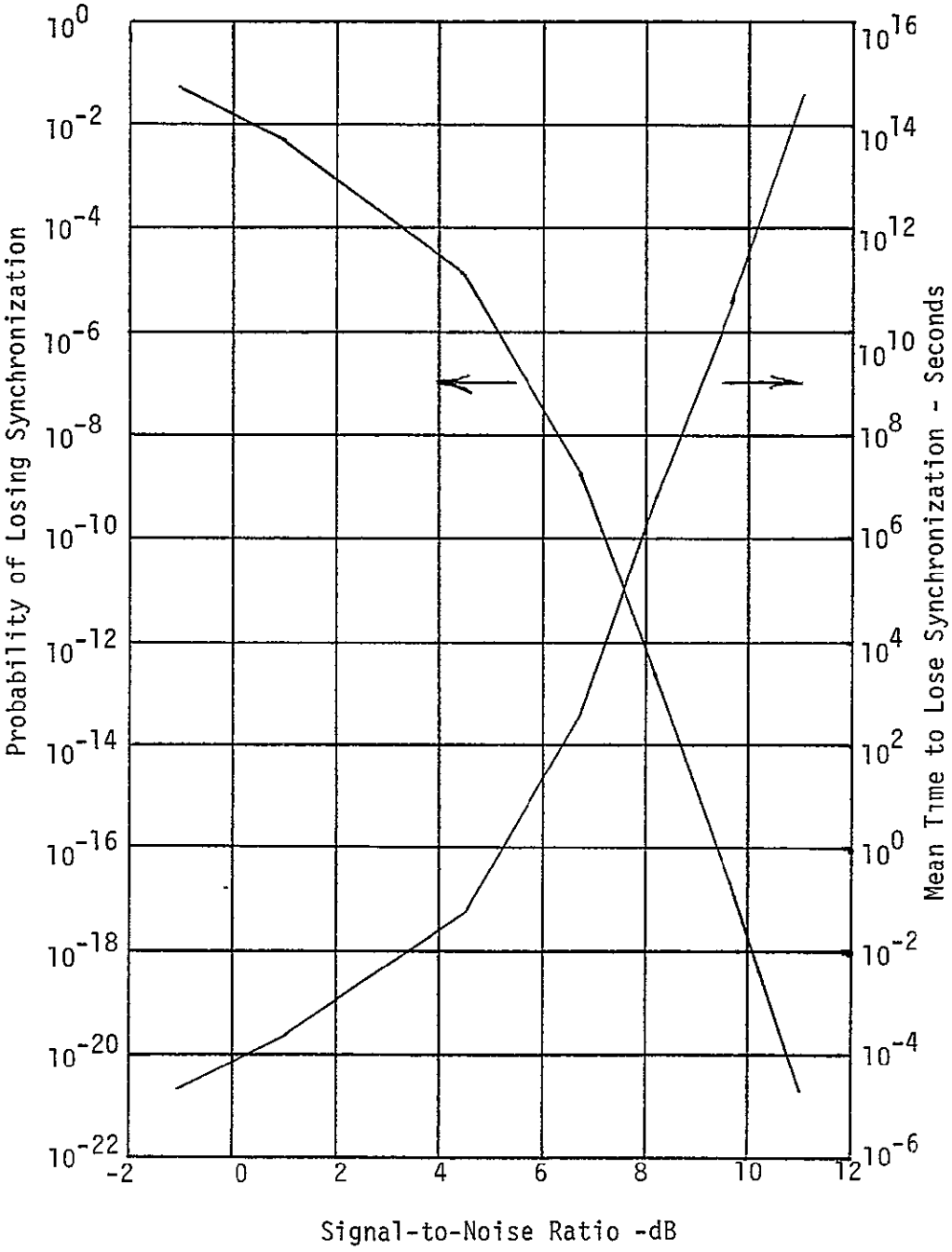


Figure E5. Probability of Synchronization Loss and Mean Time to Lose Synchronization versus Signal-to-Noise Ratio of Data

Another measure of synchronization integrity is the "mean time to lose synchronization" which is defined as the time interval in which the probability of synchronization loss occurring at least once is exactly 50%. This value can be calculated from the probability of the loop losing synchronization in a 1.6 μsec interval (P_{LS}). The probability of the circuit losing synchronization at least once in n 1.6 μsec intervals is given by

$$\text{(Prob of } \geq 1 \text{ synch loss in n intervals)} = 1 - \text{(Prob of zero synch losses in n intervals)}$$

$$= 1 - (1 - P_{LS})^n, \qquad (3)$$

which is set equal to 0.5. This is solved for n. The mean time to lose synchronization is then

$$\text{mean time to lose sync} = n \times 1.6\ \mu\text{sec} \qquad (4)$$

These values are also plotted in Figure E5 versus the data signal-to-noise ratio. From this graph it is seen that signal-to-noise ratios greater than 10 dB give mean time to unlock values greater than 10^{11} seconds (3×10^3 years). The implication of this is that the circuit will tend to maintain synchronization even if moderately noisy data is received.

An additional complication presents itself in the case of data transmitted over a biphase modulated data link (as in our system). The complication arises due to the 180° ambiquity inherent in the demodulation process. Without prior knowledge, the receiver cannot determine actual phases of data bits (0° or 180° for bipolar data), only relative phases between the data bit and some reference signal.

The result is that the receiver will output either the data as sent, or its inverse. The DDACS contains additional circuitry, in the form of an automatic data invert circuit, that decides whether the data is being received correctly or inverted and sends a signal to the Demultiplexer and D/A Converter Board to invert the data if necessary to correct it. The interface to the automatic data invert circuit is through two outputs and one input. One output (TC) is a pulse train that goes high every 1.6 μsec, whenever $\overline{TC}$ of U14 (pin 1) goes low. The other output (P_0) is a high pulse coincident with TC whenever the synchronizer slips a bit in search of proper synchronization. If synchronixation is maintained, the P_0 output is a constant low. The "invert input" is a signal which is output by the automatic data invert circuit. This signal is presented to pin 7 of the input EXCLUSIVE-OR gate (U1), and has the effect of inverting the input data if the logic level of pin 7 changes. The automatic data invert circuit is constructed using TTL logic, so the output signals are buffered with 10125 ECL-TTL converters, and the input with a 10124 TTL-ECL converter.

c) Automatic Data Invert Circuit

The automatic data invert circuit provides the DDACS with the means to decide whether the input data is the data which was sent or its inverse. If the data is being received inverted, the data invert circuit sends a signal to the demultiplexer and D/A converter board to correct the data by complementing it.

If the demultiplexer is unable to synchronize within 410 μsec (this is 4096 samples), the auto data invert circuit assumes that the incoming data is inverted, and outputs a signal to invert it back. At this point, the demultiplexer has another 410 μsec to establish synchronization, or the data will be re-inverted once again. This process continues until synchronization is established.

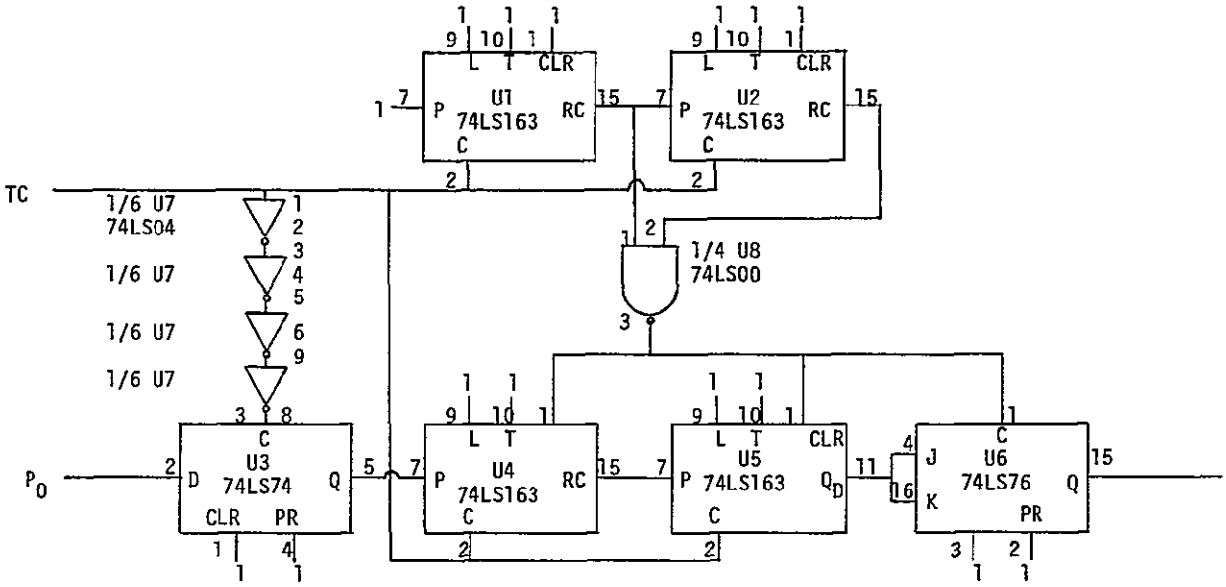


Figure E6. Schematic of Automatic Data Invert Circuit

Figure E6 shows a schematic of the automatic data invert circuit. The two inputs, TC and P_0, come from the demultiplexer board. The TC input is a pulse signal with a pulse width of 100 nsec and a pulse spacing of 1.6 μsec. One pulse occurs whenever the demultiplexer has examined 16 synchronization bits. If there have been 4 or more logic highs in that group of 16 sync bits, a high pulse will be output on the P_0 line coincident with the TC pulse. If there have been fewer than 4 highs in 16 sync bits the P_0 line remains low.

The automatic data invert circuit counts the number of P_0 pulses that occur in 255 TC pulses. If the number of P_0 pulses is a large fraction of 255 the demultiplexer is having difficulty establishing correct sync. The automatic data invert circuit assumes this is due to the complement of the correct data being

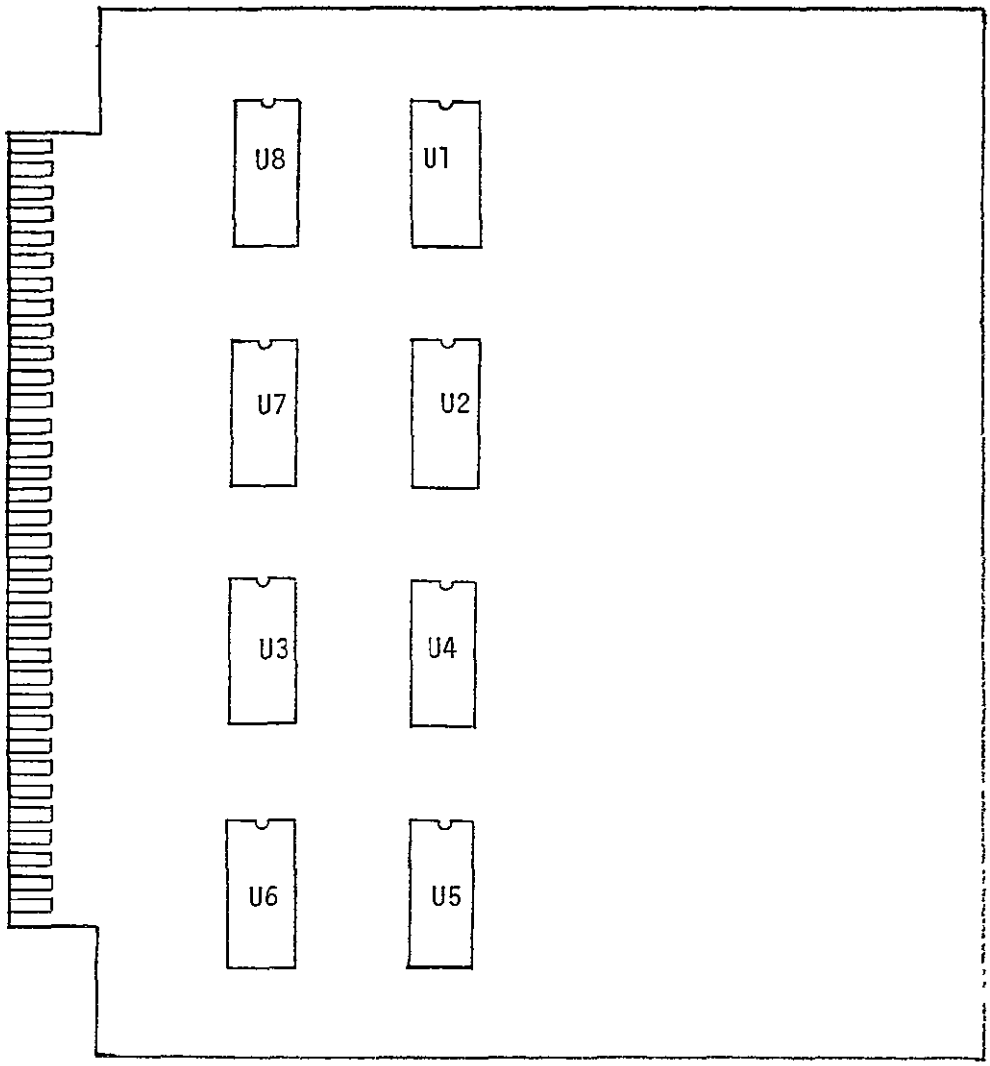
received. (It could also be due to noisy data being received). The auto data invert circuit causes the data to be inverted if 128 or greater P_0 pulses occur in 255 TC pulses.

The TC input line serves as clock for four 4-bit counters: U1, U2, U4 and U5. Counters U1 and U2 are cascaded, and count the number of TC pulses. When each counter reaches a count of "15", the RC output line (pin 15) goes high. This is detected by NAND gate U8 which puts out a low on pin 3 whenever pins 15 of both U1 and U2 are high.

Counters U4 and U5 count the number of P_0 pulses. The TC pulse, delayed 38 nsec by passing it through 4 inverters, is used to clock a 74LS74 flip-flop. The output of the flip-flop is high if a P_0 pulse is present, low if it is missing. The flip-flop output is connected to the P enable input of a pair of cascaded 74LS163 counters. When P is high, the counters increment by one with each clock pulse (TC). When P is low, the current count is maintained.

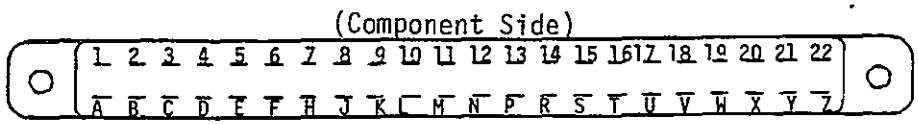
When counters U1 and U2 reach a count of 255, J-K flip-flop U6 is clocked by pin 3 of U8 (high to low transition). The output Q_D of counter U5 is connected to the J and K inputs of U6. If 128 P_0 pulses or more have been received, Q_D will be high. Otherwise Q_D will be low. Having both the J and K inputs high causes the output of U6 to toggle, which causes the data to invert at the demultiplexer board. The next TC pulse clears counters U4 and U5 and returns counters U1 and U2 to a count of zero so the process can start again. If fewer than 128 P_0 pulses have been received, Q_D will remain low. Clocking flip-flop U6 results in no change to its output state, and no subsequent inversion of the data occurs.

Figure E7 shows the physical layout of the automatic data invert circuit, and Figure E8 shows the edge card connections.



(Viewed from Component Side)

Figure E7. Physical Layout of Automatic Data Invert Circuit



Pin	Connection
1	N.C.
2	N.C.
3	N.C.
4	N.C.
5	N.C.
6	N.C.
7	N.C.
8	N.C.
9	N.C.
10	N.C.
11	N.C.
12	N.C.
13	N.C.
14	N.C.
15	N.C.
16	N.C.
17	N.C.
18	N.C.
19	N.C.
20	N.C.
21	N.C.
22	N.C.

Pin	Connection
A	GND
B	GND
C	GND
D	+5
E	N.C.
F	TC Input
H	N.C.
J	N.C.
K	N.C.
L	GND
M	N.C.
N	N.C.
P	P_O Input
R	N.C.
S	Data Invert Output
T	N.C.
U	N.C.
V	N.C.
W	N.C.
X	N.C.
Y	+5V
Z	GND

Figure E8. Edge Card Connections for Automatic Data Invert Circuit

d) Power Supplies

The power supply for the DDACS is shown schematically in Figure E9. The power requirement for the clock recovery circuit is +24 volts at 50 mA, +15 volts at 60 mA, -2 volts at 300 mA, -5 volts at 450 mA and -15 volts at 60 mA. The power requirement for the demultiplexer and D/A board is +5 volts at 120 mA, -2 volts at 1.9A, and -5 volts at 2.5A. The automatic data invert circuit requires +5 volts at 250 mA. Commercial supplies were used for the +24 and -5 volt power, while additional regulators were used to supply the +15V, +5V, -2V and -15V power. Figure E10 shows the terminal block voltages for the DDACS power distribution.

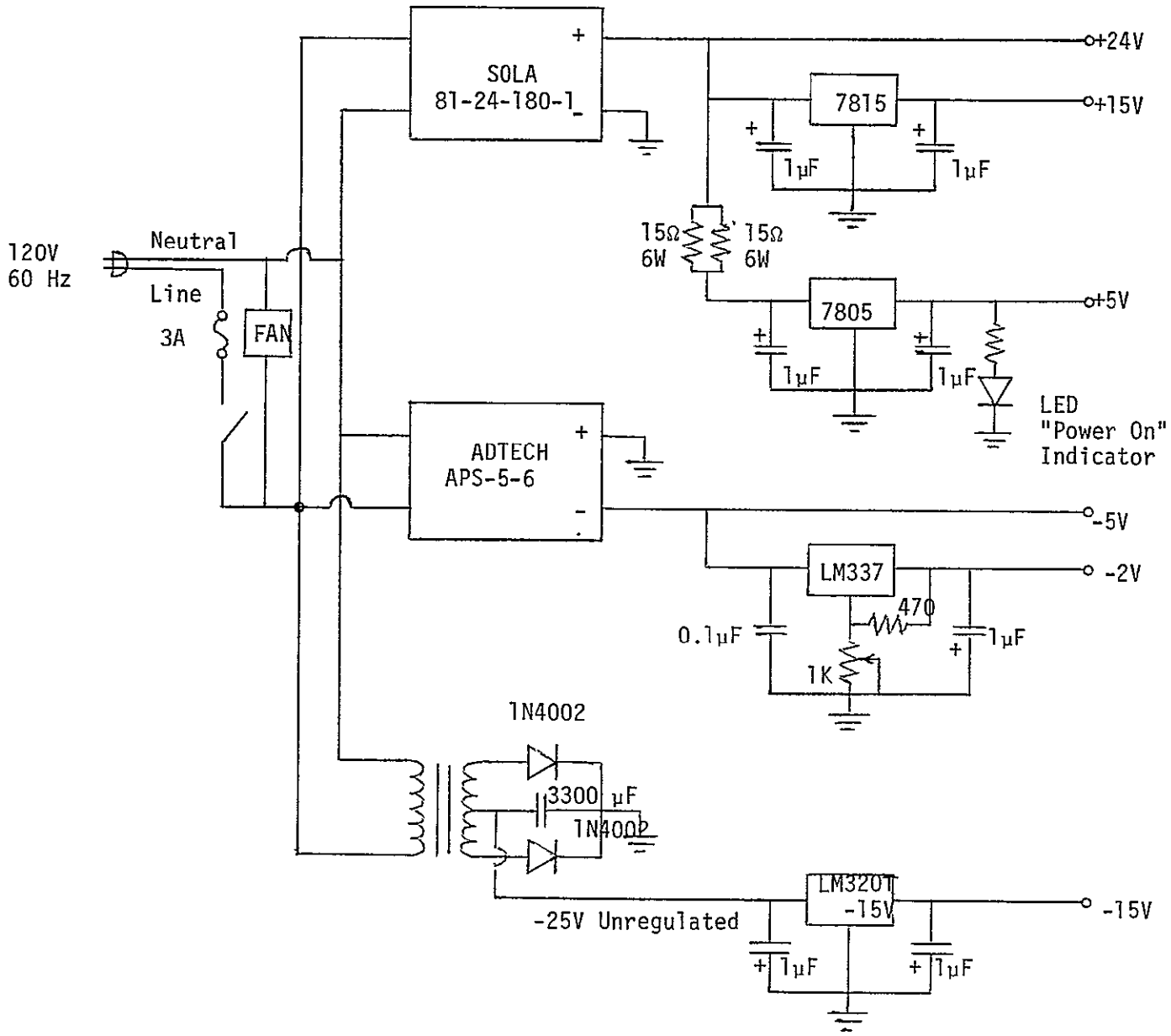


Figure E9. Power Supply Schematic for DDACS

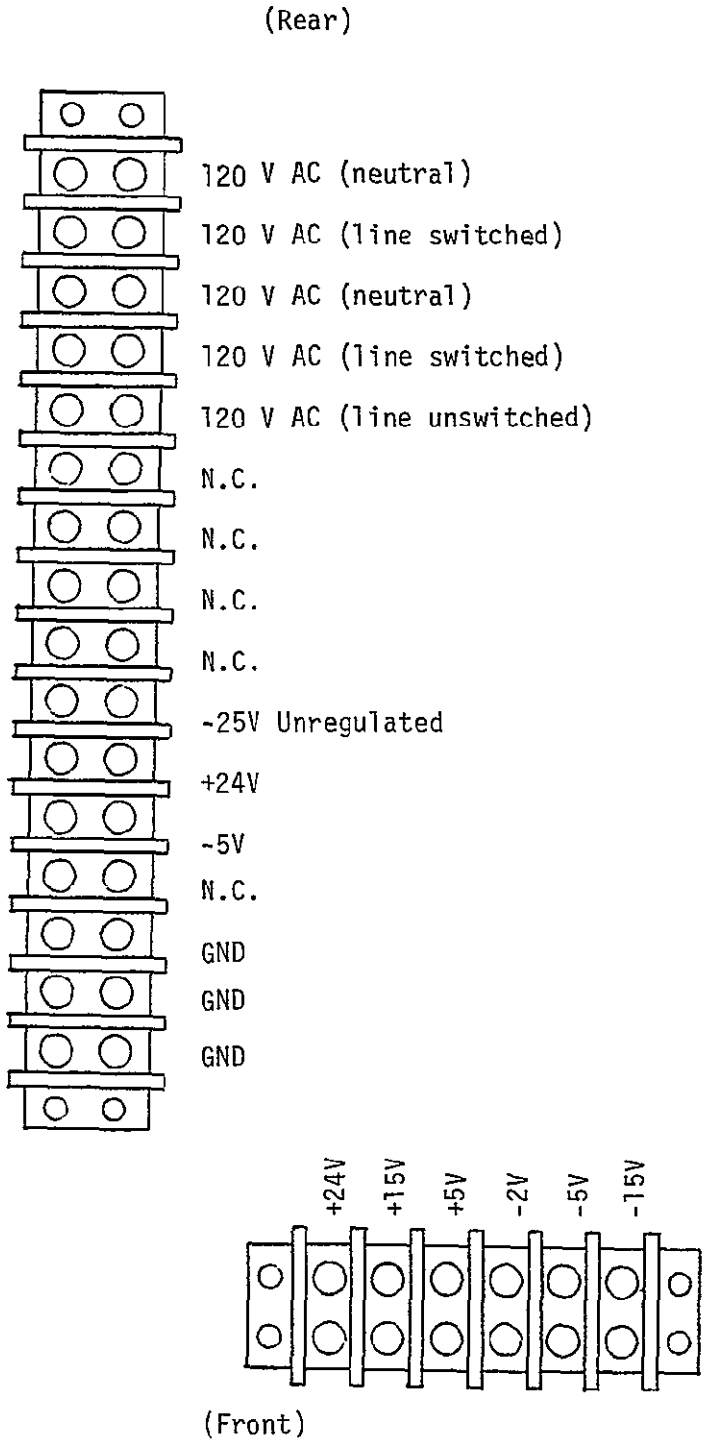


Figure E10. Terminal Block Voltages for DDACS

APPENDIX F

Data Sheets for

Transmitter and Receiver Components

CMF 4A

central microwave company

W BAND GUNN OSCILLATORS

The Central Microwave Company CMF 1200 series W band Gunn oscillator product line consists of fixed frequency mechanically trimmed sources with power levels up to 25 mW These oscillators combine Central Microwave's high performance Gunn diodes and matching cavity in a source design maximizing the performance of this combination The stability and low noise characteristics of these units make them ideally suited for service as LO s and paramp pumps

The W band source line provides ± 100 MHz smooth mechanical tuning with a frequency temperature coefficient of 2 5 MHz/°C Power stability is 0 05 dB/°C

Power input to the source is by a miniature feed-thru which is shunted internally by a Central Microwave supplied bias transient and low frequency oscillation supression circuit The body is machined from high conductivity copper with cooling provided by conduction through the UG 387/U—WR 10 mating connector

This sheet describes a basic product which will fulfill many applications Rapid response will be given to requests for custom designs requiring modification in tuning temperature range, or other parameters required to meet a specific application

ELECTRICAL CHARACTERISTICS AT 25° C

Model[1] Number	Frequency[1] Range GHz	Tuning Range MHz	Minimum Power mW	Maximum[2] Operating Voltage V	Maximum[2] Operating Current MA
CMF1207 - -	90-110	± 100	5	6	750
CMF1210 - -	90-110	± 100	10	6	900
CMF1214 - -	90-110	± 100	25	6	1200

1 The customer will supply specific center frequency in the purchase order A letter code will be added to the part number by Central Microwave to define specific units shipped This complete number should be included on re-orders

2 Oscillators will meet specification at voltage and currents equal to or less than maximum Specific values required will be supplied with each source and may vary between units

ABSOLUTE MAXIMUM RATINGS[3]

Temperature range storage	-55°C to +125°C
Temperature range, operating	-55°C to +65°C
Voltage	7V

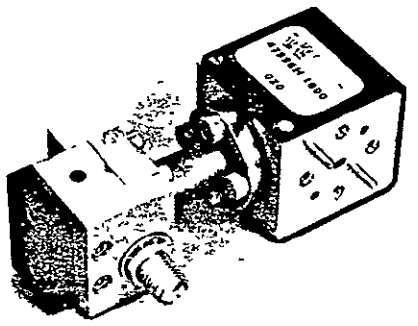
3 Exceeding these values for even transient periods may result in damage to oscillators CMF1200 series oscillators will not be damaged by operation over -55°C to +65°C temperature range, however specified power and frequency and power-frequency coefficients may only be met in the range 25 to 50°C

Specifications subject to change

JAN 1980

3701 Mueller Road ● St. Charles, Missouri 63301 ● 314-723-4700

PIN Bi-phase Modulators



Hughes PIN Bi-phase Modulators are circulator-coupled, path-length modulators that provide a 180° phase change to the signal passing through. They are available in six waveguide bands between 26.5 and 110 GHz.

The switching speed of the Hughes PIN diode enables modulation rates up to 1 gigabit-per-second. Differential phase error of less than 4° with an amplitude unbalance of 1 dB is guaranteed.

INSERTION LOSS

INSERTION LOSS (dB max)

OTHER ELECTRICAL SPECIFICATIONS

RF BANDWIDTH (% typ)	4 0
POWER HANDLING (mW max)'	100
SWITCHING TIME (10% to 90%) (ps)	<500
MAX MODULATION RATE (gigabits/sec)	>1 0
ON CURRENT (mA max)	10
OFF VOLTAGE (V max)	10
VSWR (typ)	1 3 to 1 5
DIFFERENTIAL PHASE ERROR	±2°
AMPLITUDE UNBALANCE (dB typ)	0 5
(dB max)	1 0

NOTE All specifications apply at 25°C ambient temperature

HOW TO ORDER (Specify Center Frequency at time of order)

Model Number 4799XH XOCO

Frequency Band	1 Ka 2 O 3 U 4 V 5 E 6 W
Flange Type	1 Round 2 Square (Ka band only)

EXAMPLE To order a 60GHz V Band PIN Biphase Modulator specify a Hughes Model #47994H 1000 center frequency = 60GHz

CME SERIES ELECTRONICALLY TUNED GUNN OSCILLATORS

The Central Microwave Company CME series Gunn oscillator product line consists of electronically tuned sources with power levels up to 500 mW These oscillators combine Central Microwave's high performance Gunn diodes, varactors and matching cavity in a source design maximizing the performance of this combination

Input to the Gunn diode is across two solder lugs which are shunted by a Central Microwave supplied bias transient and low frequency oscillation supression circuit A third solder lug provides varactor input The body is machined from high conductivity copper with cooling provided by conduction through the mating flange or base

This listing describes a range of standard products which will fulfill many applications Rapid response will be given to requests for custom designs requiring modification in tuning, temperature range, or other parameters required to meet a specific application The possible combination of power levels, mechanical and frequency tuning specifications are too numerous to allow a complete listing of those available Please contact Central Microwave or your local representative with your specific requirements

ELECTRICAL CHARACTERISTICS AT 25°C [3,4]

MODEL[1] NUMBER	FREQUENCY[1] RANGE GHz	TUNING RANGE MHz		MINIMUM POWER MW	MAXIMUM[2] OPERATING VOLTAGE V	MAXIMUM[2] OPERATING CURRENT mA	MAXIMUM TUNING VOLTAGE V
		MECH	ELEC				
CME310 –	4-8	500	250	10	15	500	50
CME320 –	4-8	250	100	100	15	1000	50
CME327 –	4-8	100	30	500	15	2000	50
CME410 –	8-12	500	250	10	12	500	50
CME420 –	8-12	250	100	100	12	1000	50
CME427 –	8-12	100	30	500	12	2000	50
CME510 –	12 18	500	250	10	9	600	50
CME520	12 18	250	100	100	9	1200	50
CME527 –	12 18	100	30	500	9	2500	50
CME610 –	18-26	250	150	10	8	750	50
CME620 –	18-26	150	100	100	8	1200	50
CME623 –	18-26	100	30	200	8	2000	50
CME710 –	26-40	250	100	10	6	750	50
CME720 –	26-40	100	30	100	6	1500	50
CME810 –	40-53	250	100	10	5.5	900	50
CME817 –	40-53	100	30	50	5.5	1500	50
CME910 –	54 61	Consult		10		Consult	
CME914 –	54 61	Factory		25		Factory	
CME1010 –	62 70	Consult		10		Consult	
CME1014 –	62 70	Factory		25		Factory	

3 ABSOLUTE MAXIMUM RATINGS

Temperature range, storage	–55°C to +125°C
Temperature range, operating	–55°C to +65°C
Voltage	1 1 x Vmax

Exceeding these values for even transient periods may result in damage to oscillators CM– series oscillators will not be damaged by operation over -55°C to +65°C temperature range, however, specified power and frequency and power frequency coefficients may only be met in the range 25°C to 45°C Broader temperature range units may be purchased as a special item

4 All specifications are into a load VSWR of 1 3 1 maximum Units will not be damaged working into higher VSWR, but specifications may not be met Integral isolators can be provided by Central Microwave

5

HUGHES

HUGHES AIRCRAFT COMPANY

ELECTRON DYNAMICS DIVISION

MILLIMETER-WAVE HARMONIC MIXER

TEST DATA

MODEL NO. 47436H-1002 DATE 12-17-79

SERIAL NO 010

SALES ORDER NO 44261

FREQUENCY BAND 15-110 GHz WAVEGUIDE SIZE WR-10

DIODE WAFER SERIAL NO 3585 FLANGE MIL F 3922/ 67d-010

SIGNAL FREQ GHz	LO FREQ GHz	CONVERSION LOSS dB
95.0	8.568	32
		32
		31
98.0	8.864	32
		32
		31

SEE CAUTION NOTES REVERSE SIDE

PRODUCTION SUPERVISOR

12-18-79

QUALITY ASSURANCE

COMMENTS

FINAL TEST

AGC Amplifier P/N 6210-320 S/N [illegible]

Tester [illegible]

QA [illegible]

Date [illegible]

Data taken at room temperature.

Current +15V 150 -15V 10

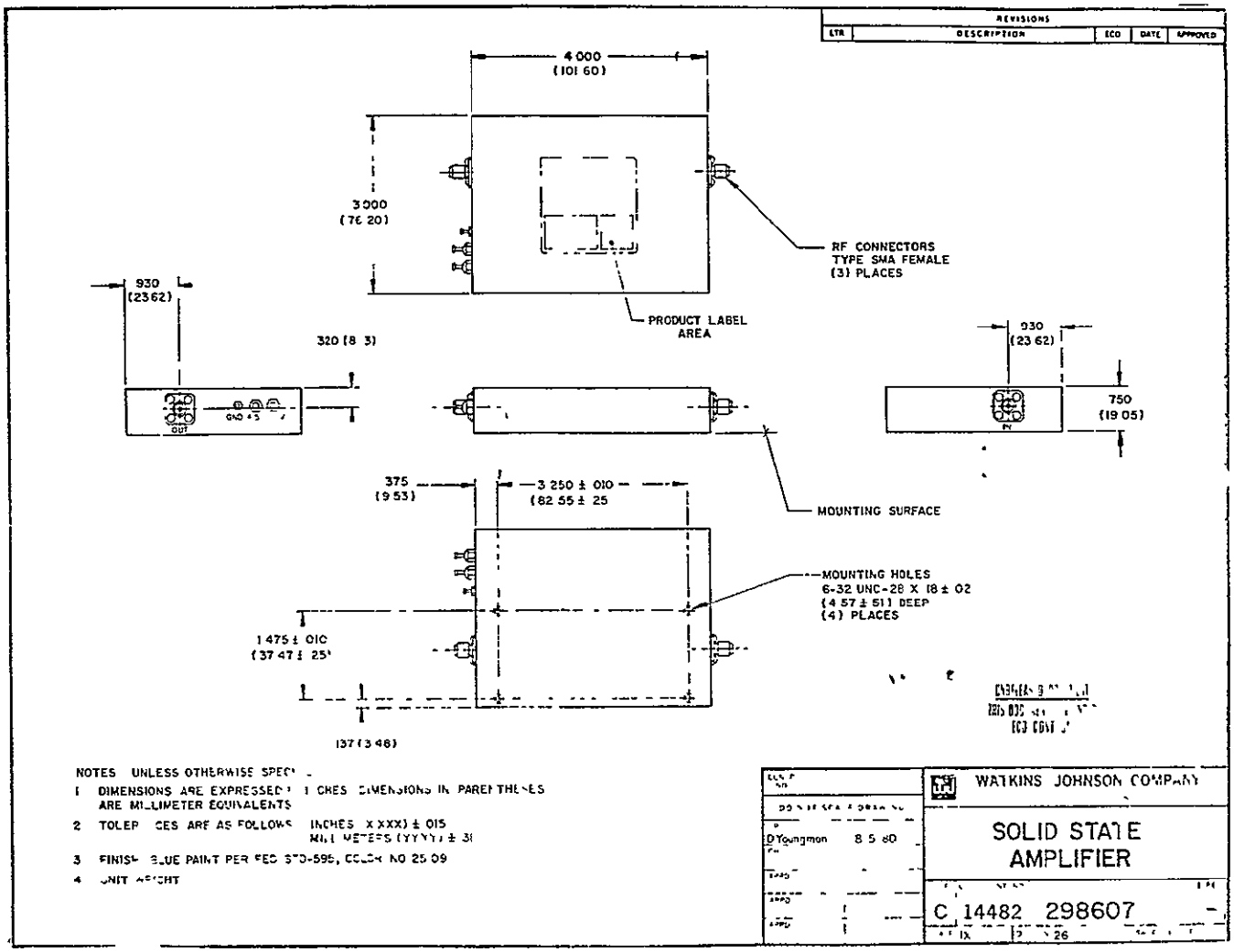
Output power 5.5 ≤ Po ≤ 9.5

Frequency 50MHz - 500MHz

Input power	Maximum output power	Minimum output power	Suppression of Strongest Harmonic	Gain (55 dB. min.)
+5dBm	7.5 dbm	6.7dbm	-26 dbc	
-20 dBm	7.5dbm	6.7dbm	-30 dbc	
- 50 dBm	7.5 dbm	6.7dbm	-30 dbc	62 db

WATKINS-JOHNSON COMPANY ELECTRON DEVICES ELECTRONIC SYSTEMS PALO ALTO CALIFORNIA	SIZE A	CODE IDENT NO 14482	DWG NO 12530
	SCALE	DIV	REV A

773-5


REVISIONS
LTR
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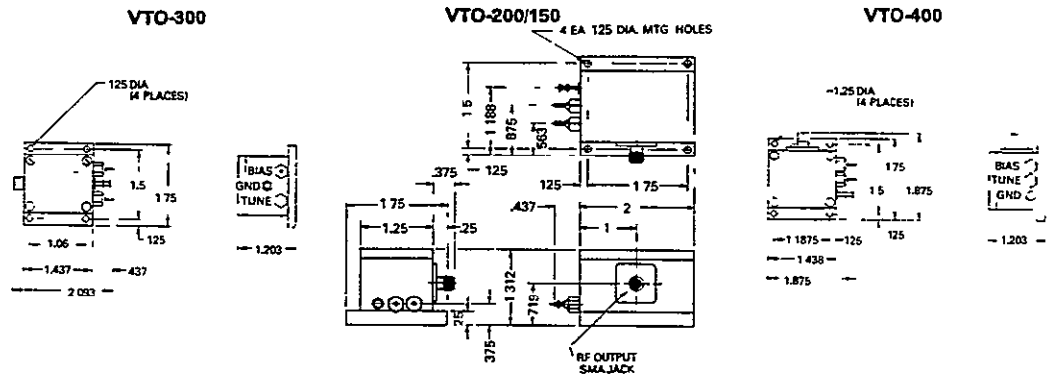
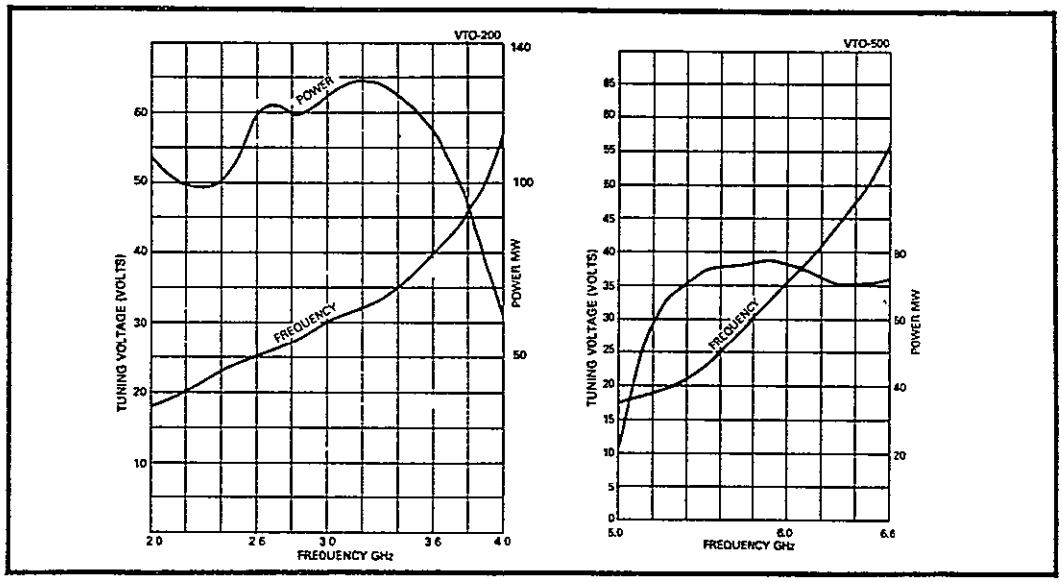
4 000
(101 60)
3 000
(76 20)
RF CONNECTORS
TYPE SMA FEMALE
(3) PLACES
PRODUCT LABEL
AREA
930
(23 62)
320 (8 3)
930
(23 62)
750
(19 05)
375
(9 53)
3 250 ± 010
(82 55 ± 25
MOUNTING SURFACE
MOUNTING HOLES
6-32 UNC-28 X 18 ± 02
(4 57 ± 51) DEEP
(4) PLACES
1 475 ± 010
(37 47 ± 25
137 (3 48)
NOTES UNLESS OTHERWISE SPEC
1 DIMENSIONS ARE EXPRESSED I CHES DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS
2 TOLERANCES ARE AS FOLLOWS INCHES X XXX) ± 015
MILLIMETERS (YYYY) ± 3
3 FINISH BLUE PAINT PER FED STD-595, COLOR NO 25 09
4 UNIT WEIGHT
D Youngmon 8 5 80
WATKINS JOHNSON COMPANY
SOLID STATE
AMPLIFIER
C 14482 298607

VTO Series





STANDARD
VTO SPECIFICATIONS

Model	Frequency Range (GHz)	Power Output (mW)	Power Variation Over Freq Range (dB)	Bias	Tuning Voltage Range	Tuning Linearity
VTO-150	1.5 to 3.0	100	6 Typ	-24 VDC @ 150 mA Typ	0 to -65 VDC	10%
VTO-200	2.0 to 4.0	50	6 Typ	-24 VDC @ 150 mA Typ	0 to -65 VDC	10%
VTO-300	3.0 to 4.0	30	6 Typ	-24 VDC @ 150 mA Typ	0 to -65 VDC	10%
VTO-400	4.0 to 5.0	25	6 Typ	-24 VDC @ 150 mA Typ	0 to -65 VDC	10%
VTO-500	5.0 to 6.0	20	6 Typ	-24 VDC @ 150 mA Typ	0 to -65 VDC	10%

All Units

Signal to Harmonic Ratio	15 dB down min 20 dB Typ
Non-Harmonic Spurious Rejection	65 dB Typ
Frequency Pulling (1.3:1 VSWR)	±2% Typ
Frequency Drift (PPM/°C)	250 Typ
Amplitude Drift (-30°C to +60°C)	1 dB Typ
Frequency Pushing	1%/Volt Typ

Opposite tuning voltage available, consult factory

Mechanical

Connectors — RF	SMA
DC	Solder Feedthru
Tuning	Solder Feedthru standard SMA for modulation

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APPENDIX G

Data Sheets on

TRW TDC1007J Monolithic Video A/D Converter

and

TRW TDC1007PCB Video A/D Converter Board

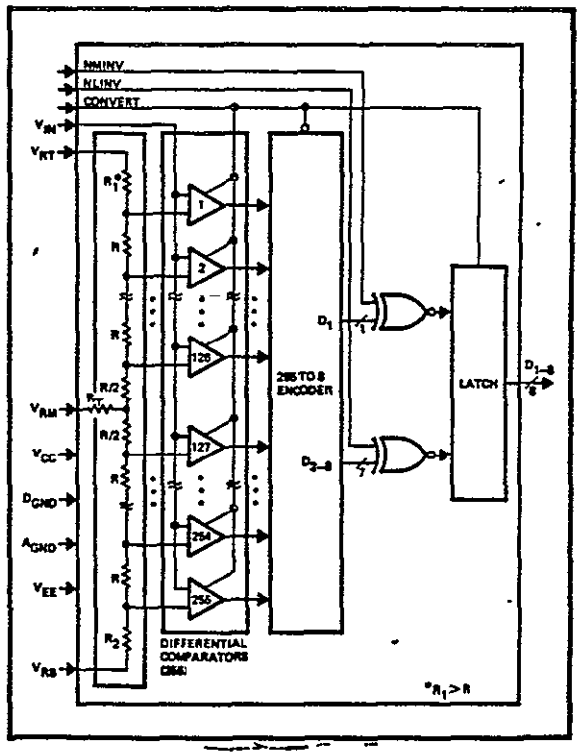
TRW | MONOLITHIC VIDEO A/D CONVERTER
8 BIT, 30 MSPS

Model: TDC1007J

The TRW TDC1007J is an 8 bit fully-parallel (flash) A/D converter capable of digitizing an analog signal at rates from dc to 30 megasamples per second (MSPS). It will accurately sample, without an external sample-and-hold circuit, input signals with frequency components up to 7 MHz (comparator 3 dB bandwidth of 40 MHz)

A single convert signal controls the unit operation, which consists of 255 sampling comparators, combining logic, and an output buffer register. Recovery from a full scale step input occurs within 20 nsec. Controls are provided for straight binary or offset two's complement output coding, in true or inverted sense

The TDC1007J is patented (No 3283170), with other patents pending. It is covered by TRW's standard 1-year limited warranty.



FEATURES

- 8 bit resolution
- 30 MSPS
- No sample-and-hold circuit required
- Aperture jitter 30 psec
- Differential phase 0.5°
- Differential gain 1.5%
- Binary or two's complement output
- Monolithic, bipolar, TTL
- 64-pin ceramic DIP
- 2.0 W power dissipation

APPLICATIONS

- Video data conversion
  - 3X or 4X NTSC color
  - 3X or 4X PAL color
- Radar data conversion
- High speed multiplexed data acquisition

TRW LSI PRODUCTS
2525 E. El Segundo Blvd., El Segundo, CA 90245
(213) 535-1831

© TRW Inc. 1978

1018–10/79

A1

'TDC1007J

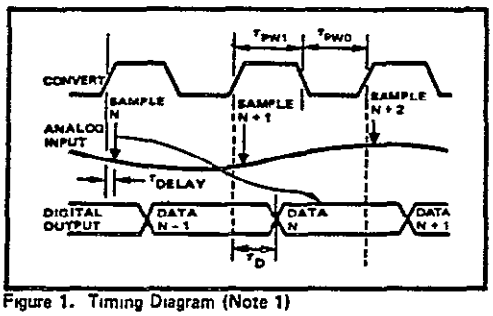


Figure 1. Timing Diagram (Note 1)

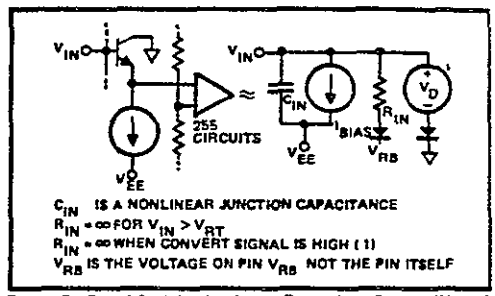


Figure 2 Simplified Analog Input Equivalent Circuit (Note 2

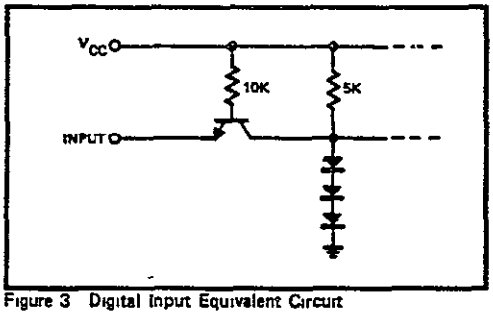


Figure 3 Digital Input Equivalent Circuit

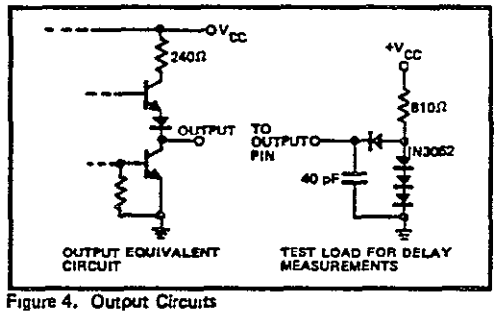


Figure 4. Output Circuits

Performance characteristics, typical over recommended operating temperature range

PARAMETER	TEST CONDITIONS		UNIT
Resolution		8 0.39	Bits %
Input Range		2 0	V
Linearity Error	0 to 20 MSPS conversion rate	0.2	%
Offset Error, Top Bottom	V_{RT} = 0 V V_{RB} = -2.0 V (Note 3) V_{RT} = 0 V V_{RB} = -2.0 V (Note 3)	+30 -24	mV mV
Aperture Jitter		30	psec
Differential Phase Differential Gain	NTSC or PAL ramp modulated with a 40 IRE color subcarrier (Note 4)	0.5 1.5	Deg %
Bandwidth 3.0 dB 0 1 dB		 40 7	 MHz MHz
Transient Response	Recovery from full scale input step	20	nsec
Signal-to-Noise Ratio Peak Signal/RMS Noise RMS Signal/RMS Noise	10 MHz bandwidth 25 MSPS conversion rate (Note 5) 1.248 MHz input 2.438 MHz input 1.248 MHz input 2.438 MHz input	 55 54 46 45	 dB dB dB dB
Noise Power Ratio	DC to 8 MHz white noise bandwidth 4σ loading 1.248 MHz slot 20 MSPS conversion rate (Note 6)	36.5	dB

TDC1007J/TDC1007J-M

COMMERCIAL AND MILITARY SPECIFICATIONS

Absolute maximum ratings (beyond which the useful life may be impaired)

Supply voltage, V_{CC} . . . . . -0.5 to +7.0 V
V_{EE} . . . . . +0.5 to -7.0 V
A_{GND} . . . . . +1.0 to -1.0 V
Input voltage, digital . . . . . -0.5 to +5.5 V
analog, V_{IN}, V_{RT}, V_{RB} . . . . . +0.5 V to V_{EE}
$|V_{RT} - V_{RB}|$ . . . . . 2.5 V
Input current, I_{IN} . . . . . +100 to -100 mA
Output voltage . . . . . -0.5 to +7.0 V
Temperature, operating, ambient . . . . . -60 to +130°C
junction . . . . . +175°C
lead soldering (10 seconds) . . . . . +300°C
storage . . . . . -65 to +150°C

Recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage (TDC1007J)	+4.75	+5.0	+5.25	V
	(TDC1007J-M)	+4.5	+5.0	+5.5	V
V_{EE}	Supply Voltage	-5.75	-6.0	-6.25	V
A_{GND}	Analog Ground Voltage	-0.1		+0.1	V
V_{RT}	Reference Input, Top	-1.1	0	+0.1	V
V_{RB}	Reference Input, Bottom	-0.9	-2.0	-2.1	V
V_{RT}-V_{RB}	Input Voltage Range	1.0	2.0	2.2	V
τ_{PW1}	Convert Pulse Width, High (Note 1)	15			nsec
τ_{PW0}	Convert Pulse Width, Low (Note 1)	25			nsec
I_{OH}	Output Current, High Level			-400	µA
I_{OL}	Output Current, Low Level			4.0	mA
T_A	Temperature, Ambient (TDC1007J)	0		+70	°C
T_C	Temperature, Case (TDC1007J-M)	-30		+125	°C

Interface specifications over recommended operating temperature range (except as noted) [1]

PARAMETER		TEST CONDITIONS	MIN	TYP*	MAX	UNIT
Power Supply						
I_{CC}	Supply Current	V_{CC} = MAX		25	35	mA
I_{EE}	Supply Current	V_{EE} = MAX $T_C \geq 0°C$		-325	-400	mA
		$T_C < 0°C$			-450	mA
Analog						
Signal Input						
V_{IN}	Input Voltage Range		V_{RT}		V_{RB}	V
R_{IN}	Equivalent Input Impedance	V_{EE} = MAX (Note 2)	5		∞	K
C_{IN}	Input Capacitance				300	pF
I_{BIAS}	Constant Input Bias	V_{EE} = MAX			500	µA
I_B	Clock Synchronous Bus	V_{EE} = MAX			200	µA
Reference Input						
I_{RT}	Reference Current, Top	V_{EE} = MAX V_{RT} = 0.0 V V_{RB} = -2.0 V			+35	mA
I_{RB}	Reference Current, Bottom	V_{EE} = MAX V_{RT} = 0.0 V V_{RB} = -2.0 V			-35	mA
R	Reference Resistor		0.22	0.31		Ω
R_T	Trim Resistor			15		KΩ
Digital						
Inputs						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	V_{CC} = MAX V_{IH} = 2.4 V			75	µA
I_{IL}	Low Level Input Current	V_{CC} = MAX V_{IL} = 0.5 V			-2.0	mA
Outputs						
V_{OH}	High Level Output Voltage	V_{CC} = MIN I_{OH} = MAX	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = MIN I_{OL} = MAX			0.5	V

Switching characteristics over recommended operating temperature range (except as noted)

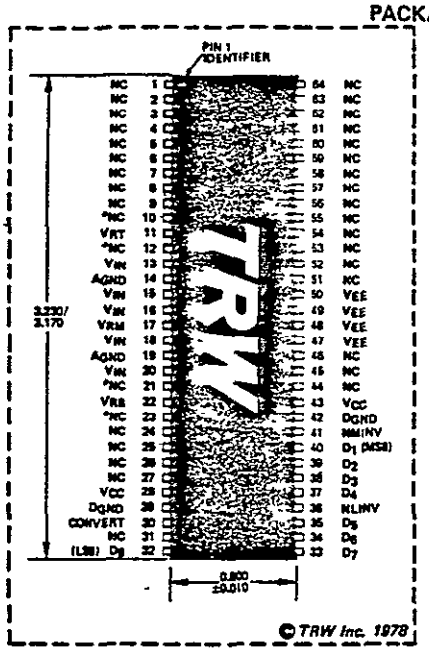
PARAMETER		TEST CONDITIONS	MIN	TYP*	MAX	UNIT
F_s	Maximum Conversion Rate	V_{CC}, V_{EE} = MIN	20	30		MHz
τ_{DELAY}	Aperture Delay (Note 1)	V_{CC}, V_{EE} = MIN		10		nsec
τ_D	Digital Output Delay (Note 1)	V_{CC}, V_{EE} = MIN	15	30	45	nsec

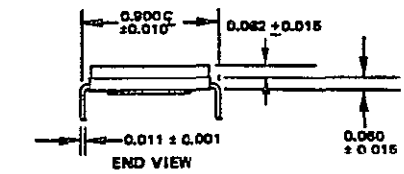
*V_{CC}, V_{EE} = NOM T_A = 25°C All voltages measured with respect to D_{GND}.
[1]Test Conditions. V_{CC}, V_{EE}, V_{RT}, V_{RB} = NOM (Except as Noted)
All measurements under D C conditions

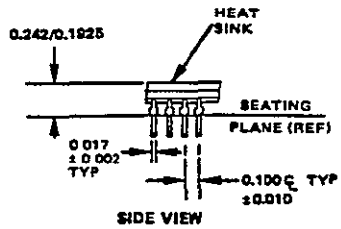
TRW LSI PRODUCTS

TDC1007J

PACKAGE INFORMATION







NOTES
- DIMENSIONS IN INCHES
- ALL POWER AND GROUND PINS MUST BE CONNECTED
- DGND IS +5V GROUND AND REFERENCES TTL I/O BUFFERS ONLY
- ALL V_{IN} PINS MUST BE EXTERNALLY CONNECTED

*RECOMMENDED CONNECTION TO ANALOG GROUND FOR INTERELECTRODE SHIELDING

MATING CONNECTORS INCLUDE:

Cambion	703-4064-01-04-12	Low-profile, solder tail, tin plate, jam socket
Robinson-Nugent	ICN-649 S5-G	Low-profile, solder tail, gold plate, jam socket
Textool	232-2601-00-0605 (2 required)	Solder tail, nickel plate, zero insertion force socket

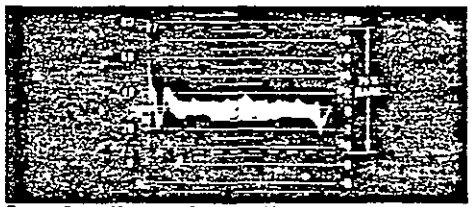


Figure 5. Differential Phase – 40 IRE Modulated NTSC Ramp – 14.3 MSPS Unlocked (Note 4)

Figure 6. Differential Gain – 40 IRE Modulated NTSC Ramp – 14.3 MSPS Unlocked (Note 4)

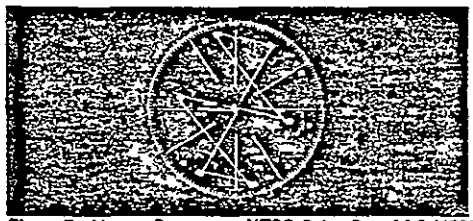


Figure 7. Vector Diagram – NTSC Color Bars 14.3 MSPS Unlocked (Note 4)

Figure 8. Linearity – 20 MSPS (Note 7)

TRW LSI PRODUCTS

A4

OUTPUT CODING

STEP	RANGE		BINARY		OFFSET TWO's COMPLEMENT	
			TRUE	INVERTED	TRUE	INVERTED
	2 0000V FS 7.8431 mV STEP	-2 0480V FS 8 000 mV STEP	NMINV = 1 NLINV = 1	0 0	0 1	1 0
000	0.0000V	0 0000V	00000000	11111111	10000000	01111111
001	0.0078V	0.0080V	00000001	11111110	10000001	01111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	0.9961V	-1 0160V	01111111	10000000	11111111	00000000
128	-1 0039V	-1 0240V	10000000	01111111	00000000	11111111
129	-1 0118V	-1 0320V	10000001	01111110	00000001	11111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
254	-1.9921V	-1 9992V	11111110	00000001	01111110	10000001
255	2 0000 V	-2.0400 V	11111111	00000000	01111111	10000000

NMINV and NLINV are to be considered DC controls They may be tied to +5V for a logical '1' and tied to ground for a logical '0'.

NOTES

1. Timing The TDC1007J operation involves a 1 bit pipeline delay. A sample is taken (comparators are latched) approximately 10 nsec after the rising edge of the convert signal (τ_{DELAY}). This delay may vary by a few nanoseconds from part to part and as a function of temperature, but the short-term uncertainty (jitter) in strobe delay is less than 30 psec. The 255 to 8 encoding is performed on the falling edge of the convert signal, and the result is transferred to the output latches on the next rising edge. The outputs require a minimum time to begin changing to the new result, specified as $\tau_{D(min)}$. This permits the preceding result to be read on the same rising edge, i.e , read data N while acquiring sample N+2.

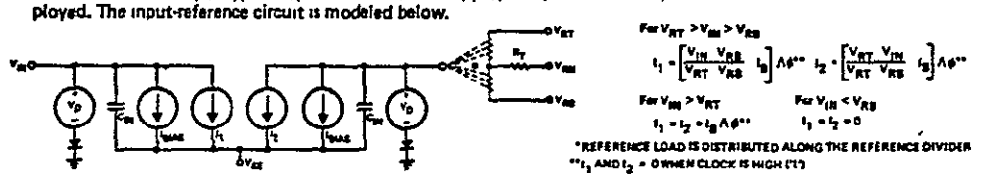
   The specified minimum convert pulse widths(τ_{PW1}, τ_{PW0}) guarantee performance of all parts over the full operating temperature range. They can be adjusted to smaller widths for a particular part, achieving the typical sample rate. All timing specifications are with respect to TTL threshold crossing (1.5 V).

2. Analog Input. The analog input circuit of Figure 2 is a simplification that is adequate for most interface circuit designs As shown, the input consists of 255 parallel emitter-follower stages driving voltage comparators C_{IN} represents the nonlinear emitter-follower junction capacitance, and I_{BIAS} is the constant input bias current. R_{IN} is a piecewise linear approximation of the change in input current due to comparator switching as the input moves through the range. This component does not vary after the input range is exceeded, as no additional comparators can be switched, but do note that the comparator current is zero (R^{∞}) while the convert signal is high ('1'). The diode voltage in the model represents the base-collector junctions of the emitter-follower transistors, which can conduct if the input exceeds +0.7V.

   The 300 pF maximum input capacitance presents a drive requirement similar to that of a 75 ohm coaxial cable, through its nonlinear nature and dc bias characteristics make it unsuited to being driven directly by a 75 ohm line: A source impedance of less than 10 ohms is indicated for optimal performance. One method of providing this drive is demonstrated on the TDC1007PCB (page 9). This is not necessarily the best or most cost effective technique. The LH0033, or equivalent, buffer amplifier also works, and common analog line driver circuits can be adapted to the task. Through the use of NMINV and NLINV, either inverting or noninverting buffers may be accommodated.

3. Reference Inputs. The resistive divider that provides a reference voltage to each of the 255 comparator circuits has both ends and a midpoint tap available to the user, allowing considerable flexibility in the circuit operation. The nominal operating range is 0 to -2V, requiring approximately 0V on V_{RT} and -2V on V_{RB} This is not to preclude operation over a smaller range, as the circuit will function with a total range of less than 1 volt, but some performance characteristics will change. For example, a quantizer circuit has two major sources of dc linearity error: resistor ladder variations and comparator offset voltages. The former is scaled by a range reduction while the latter is not. The circuit should be operated with V_{RT} and V_{RB} within the recommended +0.1 to -2.1V range, and V_{RB} at least 800 mV more negative than V_{RT}.

   When one of the 255 comparators turns off due to a drop in analog input voltage, its bias current shifts from the analog input to the reference ladder. When the convert signal is high, comparator bias current is zero. This generates clock and signal related current noise on the reference inputs with a maximum amplitude of I_B, which can be relieved by ensuring adequate bypassing of V_{RT} and V_{RB} to analog ground. If the reference inputs are exercised dynamically, as in an AGC circuit, a bypass capacitor would be inappropriate, and a low impedance reference source should be employed. The input-reference circuit is modeled below.



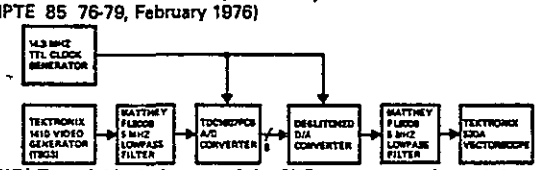
TDC1007J

Reference Inputs (Cont.)

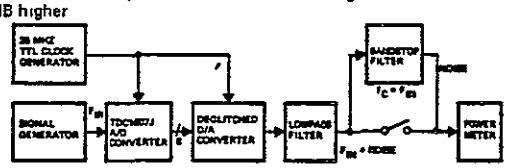
Calibration is accomplished by adjusting V_{RT} and V_{RB} to set the first and 255th thresholds to the desired voltages Note that R_1 is greater than R, ensuring that calibration can be achieved with a positive voltage on V_{RT} Assuming a 0 to -2V desired range, continuously strobe the converter with -0 0039V on the analog input, and adjust V_{RT} for output toggling between codes 000 and 001. Then apply -1.9961V and adjust V_{RB} for toggling between codes 254 and 255 Rather than adjusting V_{RT}, it may be convenient to connect it to analog ground and calibrate the 0V end of the range with a buffer offset control V_{RB} is a convenient point for gain adjust that is not in the analog signal path These techniques are employed on the TDC1007PCB (page 7)

A midpoint tap, V_{RM}, allows the user to parallel the upper or lower half of the ladder with a trim resistor, R_T This produces approximately 1/2 LSB adjustment of the linearity midpoint and is included for linearity compensation of an extended temperature version of this part. It is not necessary that adjustment be performed over the commercial temperature range (0 to 70°C) This pin can also be useful as a virtual ground reference for the input buffer amplifier if bipolar conversions are performed. (Be aware of the inherent R_T impedance of this node) Any load applied to V_{RM} will affect linearity

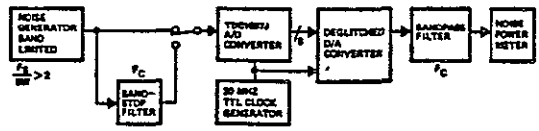
4. **NTSC Video Testing.** Measurment of video test signals is performed using the setup illustrated The A/D and D/A converters are strobed at 14.3 MHz, unlocked from the color subcarrier, and the full composite signal encoded No (sin x)/x correction is performed. Differential phase and gain, in excess of that inherent in 8 bit quantization, are determined by measuring the deviation of the trace centerline on a vectorscope monitoring a reconstructed 40 IRE modulated ramp, sampled asynchronously with the color subcarrier (M O. Felix, "Differential Phase and Gain Measurements in Digitized Video Signals," Jour. SMPTE 85 76-79, February 1976)



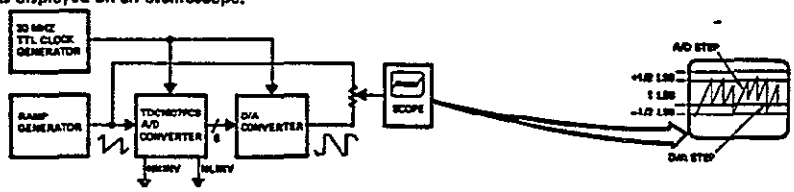
5. **Signal-to Noise Ratio (SNR) Test.** A block diagram of the SNR test setup is shown below. The analog input to the A/D converter is a single tone with a p–p amplitude equal to the full scale range of the A/D. Power in the reconstructed waveform is measured over a selected bandwidth ($< f_S/2$) and remeasured when the fundamental tone frequency is filtered out at the D/A output. The ratio of the two power readings in the SNR. An ideal A/D converter has a SNR equal to 6n + 1.8 dB, where n = number of bits, n > 4. This is the RMS signal-to-RMS noise value Peak signal-to-RMS noise theory is approximately 9 dB higher



6. **Noise Power Ratio (NPR) Test.** A block diagram of the NPR test setup is given below Bandlimited gaussian noise is the analog input to the A/D converter. Power in the reconstructed waveform is measured in a selected frequency slot and then remeasured with the same frequency slot notched out of the input signal spectrum. The ratio of the two power readings reflects the noise performance, dynamic nonlinearity of the A/D, and aperture effects. The theoretical NPR for the test performed is 40.5 dB.



7. **Linearity Testing** Device linearity is readily determined with the test setup below. The A/D output is inverted using the NMINV and NLINV controls. The input is slightly overdriven with a slow ramp, the output and input are summed, and the results displayed on an oscilloscope.



TRW LSI PRODUCTS

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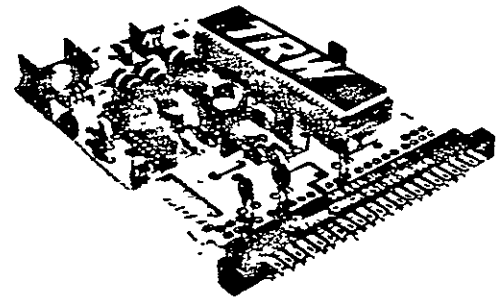
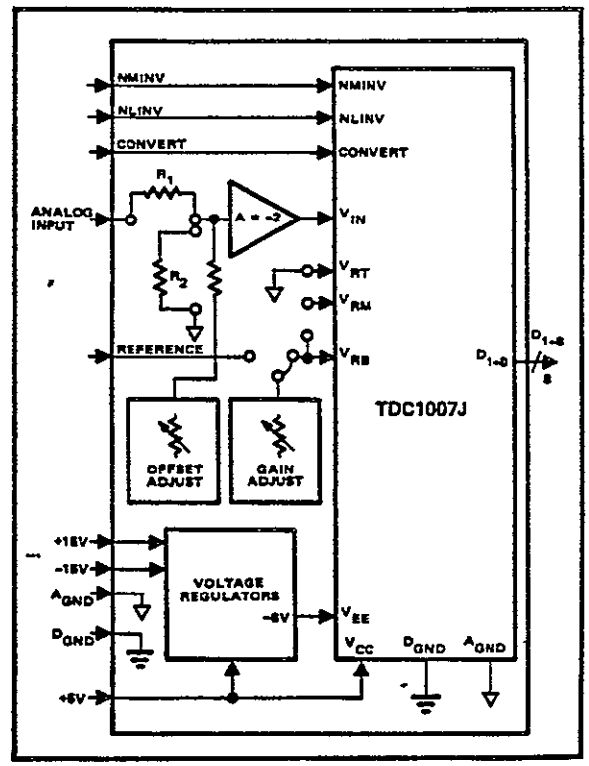
TRW | VIDEO A/D CONVERTER EVALUATION BOARD

Model: TDC1007PCB



The TRW TDC1007PCB is a fully assembled and tested circuit board designed to aid in evaluating the TDC1007J video A/D converter It comes complete with the converter LSI installed in a socket and will accept and digitize a 1 V p-p 75 ohm signal Other ranges and impedances may be selected by plug-in resistor substitutions on the board An offset adjustment is provided which can establish a unipolar or bipolar input range The circuit operates from ±15 and +5V supplies

This board is intended as a demonstration vehicle It will enable the potential user to exercise the converter with a minimum effort and demonstrates a technique of input buffering Full size prints of the board layout are included (page 11). It is equivalent to most familiar modular type video A/D converters. All digital signals are TTL compatible and are brought directly off the board from the LSI Provisions are made on the board to install a zero insertion force LSI socket for use as a test fixture



FEATURES

- Selectable input impedance
  50, 75, 93, 1 K ohms
- Selectable input range
  1, 2, 5, 10 volt full scale
- Adjustable offset for unipolar or bipolar input
- Will accommodate zero insertion force LSI socket
- ±15 V, 5% and +5 V, 10% power supplies required

APPLICATIONS

- TDC1007J evaluation
- System prototyping
- Test fixture

TRW LSI PRODUCTS

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TDC1007PCB

The principal function performed by the PCB is buffering the TDC1007J input and matching it to the source impedance. The amplifier circuit has a gain of -2 and an input impedance of 1K ohm. A resistive divider input is provided to achieve other ranges and impedances. An offset voltage is applied to the summing node to permit zero scale calibration, and the range of adjustment is sufficient for bipolar operation. Drive current to the LSI comes from an emitter-follower stage (Q1) with 60 mA bias current. C_2 and R_{10} are amplifier compensation components, and are selected at the time of assembly.

A single 2.5 volt reference (U4) serves amplifier offset, converter reference, and supply regulation functions. The ladder bottom reference is supplied by U3 and Q4, and is adjustable via a multiturn pot for full scale calibration. A trace leading to connector pin F is provided which can be used to monitor V_{RB} by connecting pad 25 to 24 as well as 23. V_{RB} can also be supplied through this pin by connecting pad 25 to pad 24 only. This can be used as a gain control, as in an AGC circuit. A 10 μF capacitor is tied from V_{RB} to ground to bypass clock and data synchronous current noise generated on the chip. If this is removed to improve the gain control response, a low impedance source must be employed. The V_{RB} input requires a 30 mA sink capability from the analog ground.

A -6 volt supply is developed by U3 and Q2, and supplies the A/D converter (U1) and buffer amplifier (U2). The +12 volt supply (U3, Q3) provides isolation between the amplifer and ±15 volt supply. The on-board regulation allows the PCB to operate from +5 percent +15V and ±10 percent +5V supplies. Maximum supply currents are 125 mA at +5V, 50 mA at +15V, 500 mA at -15V. The board can be modified to operate on ±12V instead of ±15V by bypassing the +12V regulator. This is accomplished by removing Q3, R16, and R21, and adding a jumper between Q3 emitter and collector pads.

The separate plans for analog and digital ground should be noted. A_{GND} is the return for the ±15 volt supplies and a small amount of +5 volt current. All 5 volt current supporting the digital interface is returned via the D_{GND} plane and pins; this ground separation is maintained on the chip. Good analog circuit design dictates that the ground currents be kept separate as much as possible, connected at only one point (usually the power supplies). Clock noise on the analog input can usually be traced to coupling of the ground circuits.

The LSI digital outputs are designed to drive the test load of Figure 4. This is roughly equivalent to two standard or Schottky loads or 10 low power Schottky loads. It is recommended that the LSI not drive long interconnects directly, as the line capacitance may result in excessive rise times, and reflections can contribute to noise within the converter.

INPUT RESISTOR SELECTION
(1/8W unless otherwise specified)

$$R_2 = \frac{.1}{\frac{V_{RANGE}}{Z_{IN}} - 0.001} \qquad R_1 = Z_{IN} - \frac{1000\,R_2}{1000 + R_2}$$

INPUT IMPEDANCE		INPUT RANGE			
		1V	2V	5V	10V
50Ω	R_1	0	24.9	40.2 1/2W	45.3 2W
	R_2	52.3	24.3	10 0	4.99 1/4W
75Ω	R_1	0*	37.4	60.4 1/4W	68 1 2W
	R_2	80 6*	39.2	15.4	7.50
93Ω	R_1	0	46.4	75.0 1/4W	84.5 1W
	R_2	102	48.7	19.1	9.31
1000Ω	R_1	0	499	806	909
	R_2	OPEN	1000	249	110

*75Ω 1V option supplied

TRW LSI PRODUCTS

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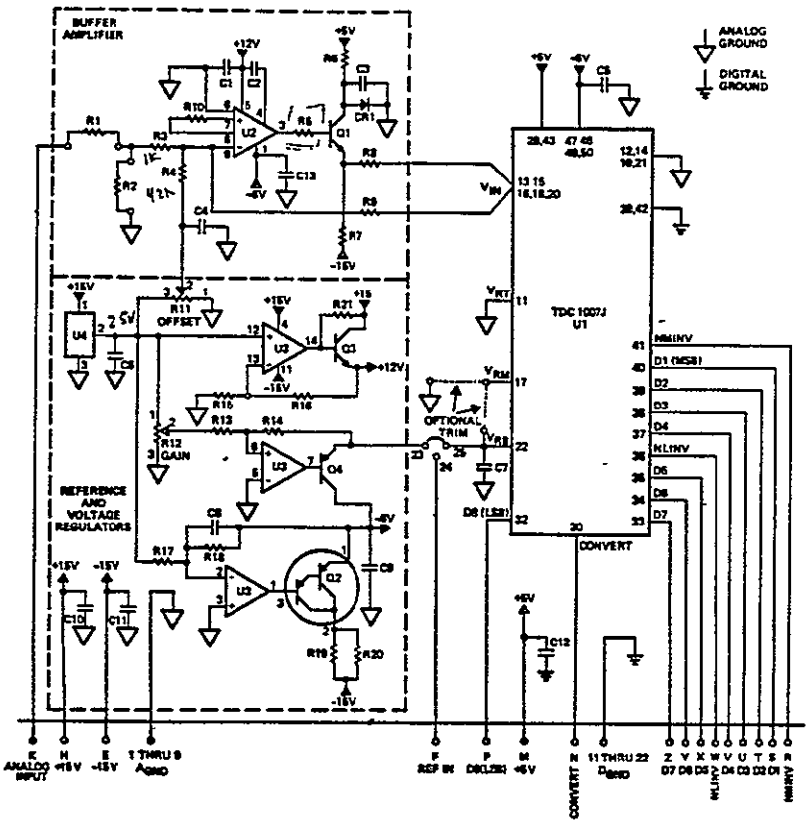
TDC1007PCB



TDC1007PCB Schematic

PARTS LIST

RESISTORS

R1	0Ω*	1/4W	2%
R2	80.6	1/4W	2%
R3	1.0KΩ	1/4W	2%
R4	4.2KΩ	1/4W	2%
R5	10Ω	1/4W	2%
R6	56Ω	1/4W	5%
R7	240Ω	2W	5%
R8	6.8Ω	1/2W	5%
R9	2.0KΩ	1/2W	2%
R10	†	1/4W	2%
R11	2.0KΩ	1/4W	Multiturn Cermet Pot
R12	2.0KΩ	1/4W	Multiturn Cermet Pot
R13	21.5KΩ	1/4W	2%
R14	21.5KΩ	1/4W	2%
R15	11.3KΩ	1/4W	2%
R16	42.2KΩ	1/4W	2%
R17	21.5KΩ	1/4W	2%
R18	51.5KΩ	1/4W	2%
R19	24Ω	2W	10%
R20	24Ω	2W	10%
R21	392Ω	1/4W	2%

CAPACITORS

C1	0.1µF	50V
C2	2.0pF†	50V
C3	0.1µF	50V
C4	0.1µF	50V
C5	0.1µF	50V
C6	1.0µF	10V
C7	10.0µF	10V
C8	0.001µF	50V
C9	100.0µF	10V
C10	10.0µF	20V
C11	10.0µF	20V
C12	10.0µF	10V
C13	0.1µF	50V

TRANSISTORS

Q1	2N5836
Q2	2N5034
Q3	2N2222
Q4	2N2907

DIODE

CR1	1N4001

MISCELLANEOUS

A1	Cambion 64 pin socket 704-4064-01-04-12 for U1**
A2	Thermalloy heat sink 60738 FOR Q2
A3	TRW Cinch edge connector 251 22 30 160
A4	Printed circuit board TRW TPC 1007
A5	Moore Systems stitch weld pins 700508 for R1, R2 (4 Required)

INTEGRATED CIRCUITS

U1	TRW TDC1007J
U2	Plessey SL541C
U3	Motorola MC4741
U4	Motorola MC1403U

*Input impedance and range select (75Ω, 1V option supplied)

**A zero insertion force socket (Textool PN 232 2501-00-0606, 2 required) may be substituted by the user

†Amplifier compensation components

TRW LSI PRODUCTS

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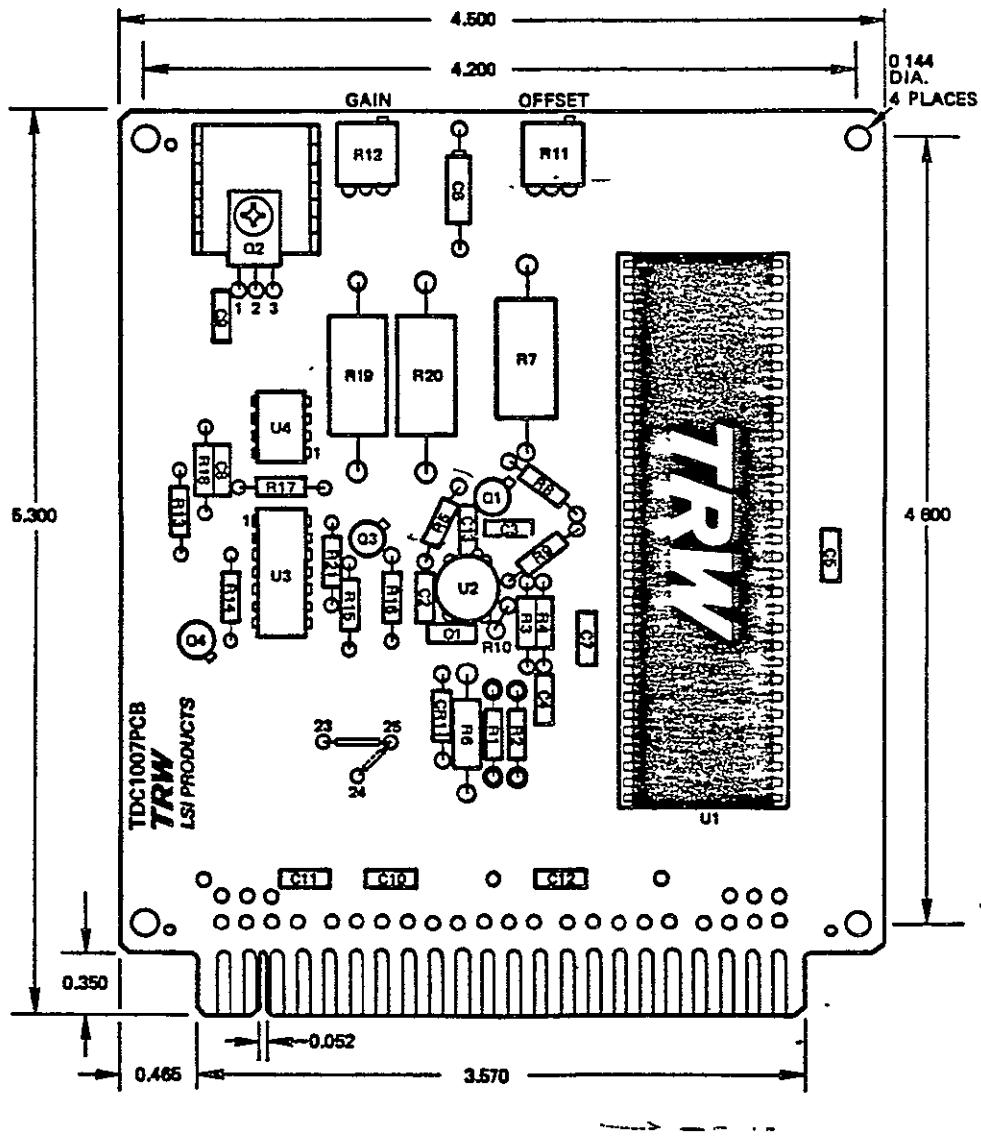
TDC1007PCB



Note: All dimensions in inches

TRW LSI PRODUCTS

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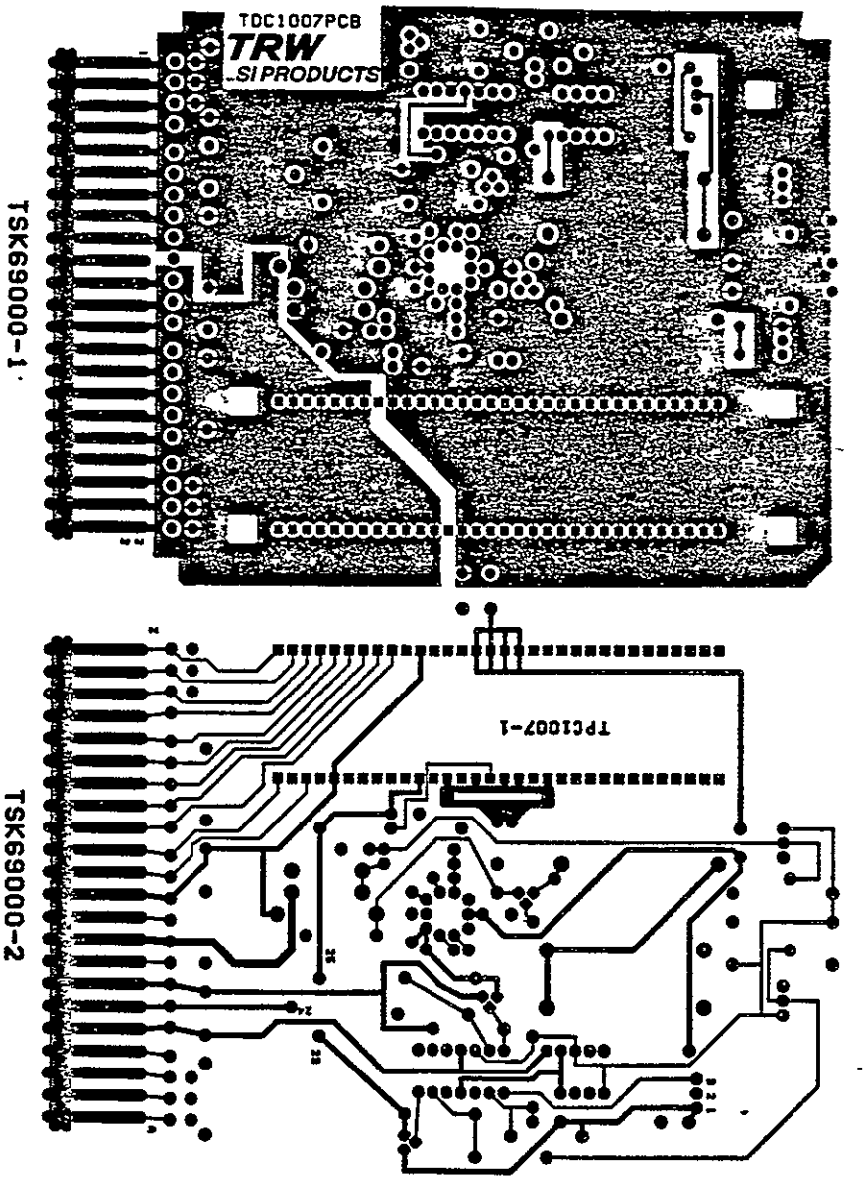
TDC1007PCB



TSK69000 – Evaluation Printed Circuit Board Layout (1X) (A 1X Mylar print is available on request)

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TRW LSI PRODUCTS

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APPENDIX H

Schematic Diagrams of

Antenna Feed

Multiplexer Circuit,

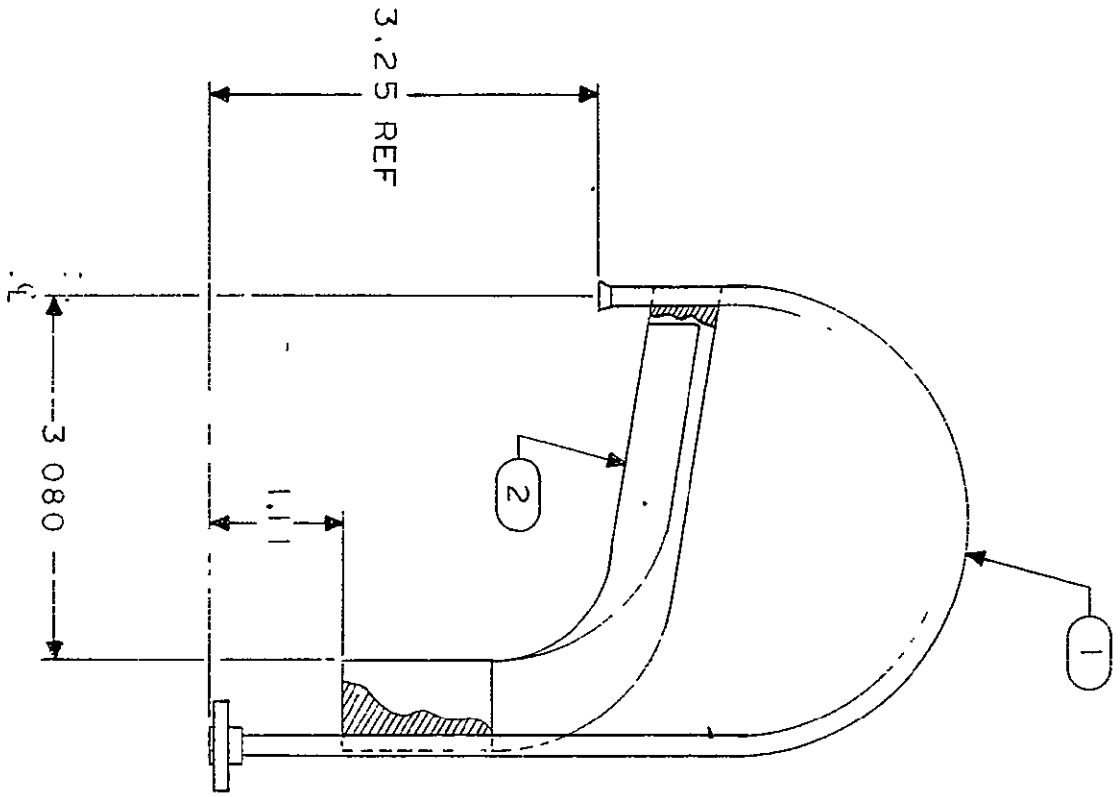
Clock Recovery Circuit,

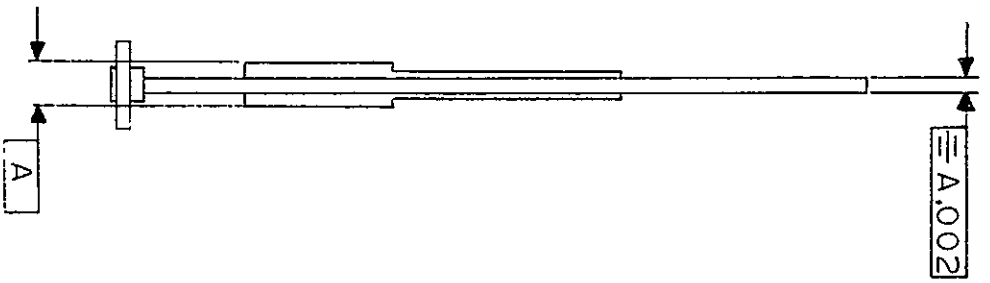
Demultiplexer, D/A Converter Circuit,

and

If amplifier strip/demodulator circuit

PN Code Generator


3.25 REF
3.080
1.11
2
1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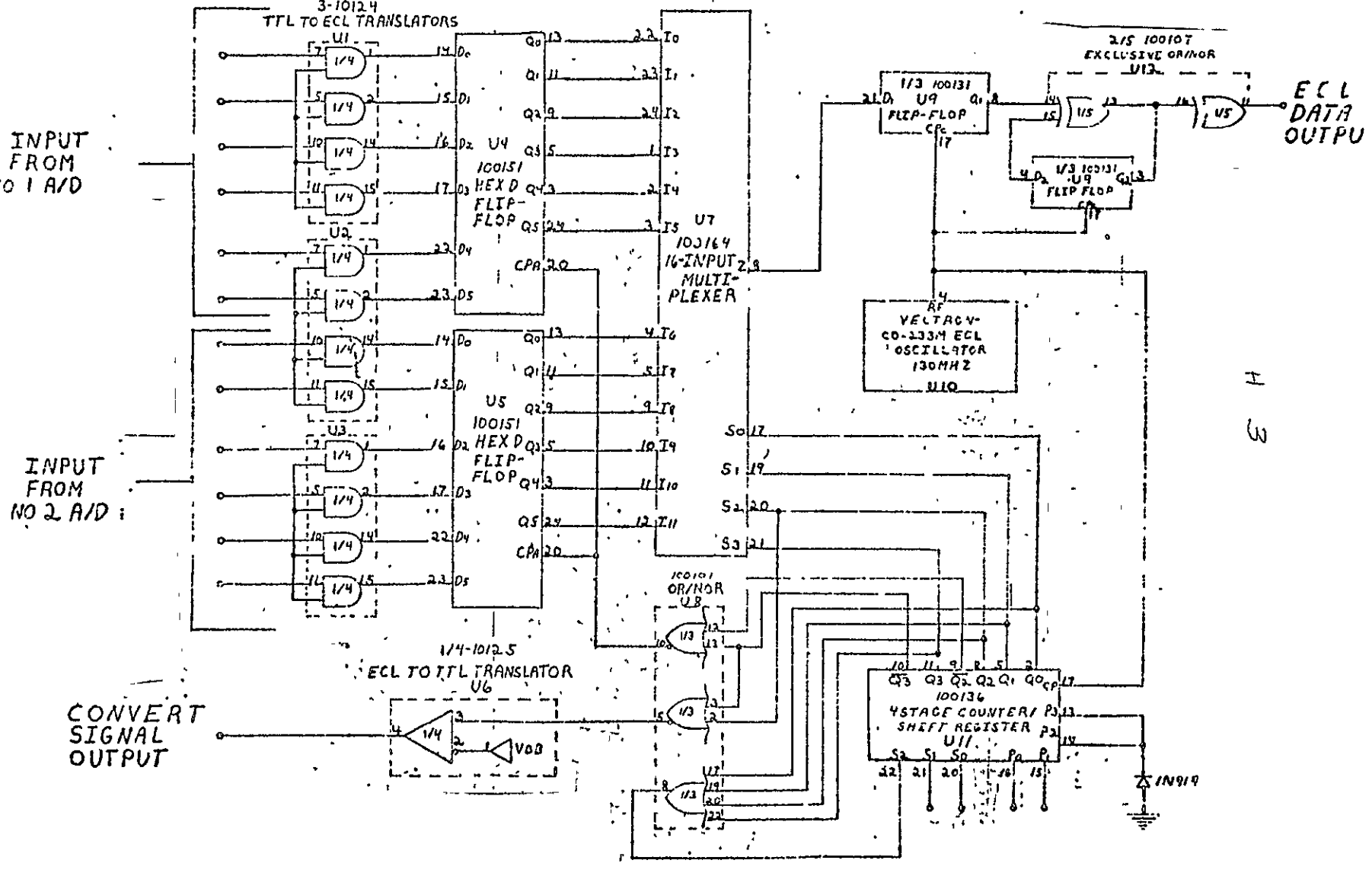
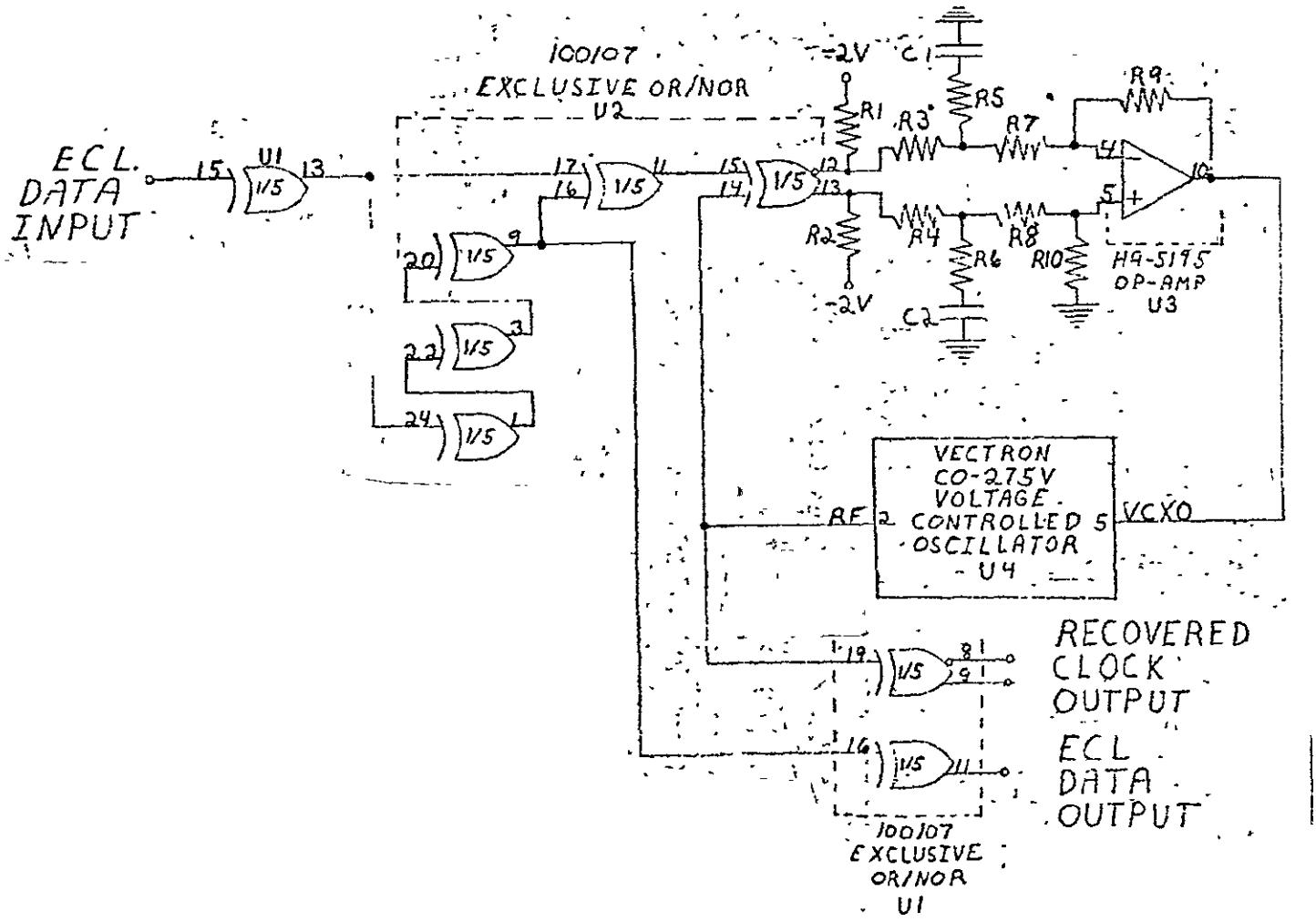
MULTIPLEXEXER/DIFFERENTIAL ENCODER SCHEMATIC

DRAWING 1

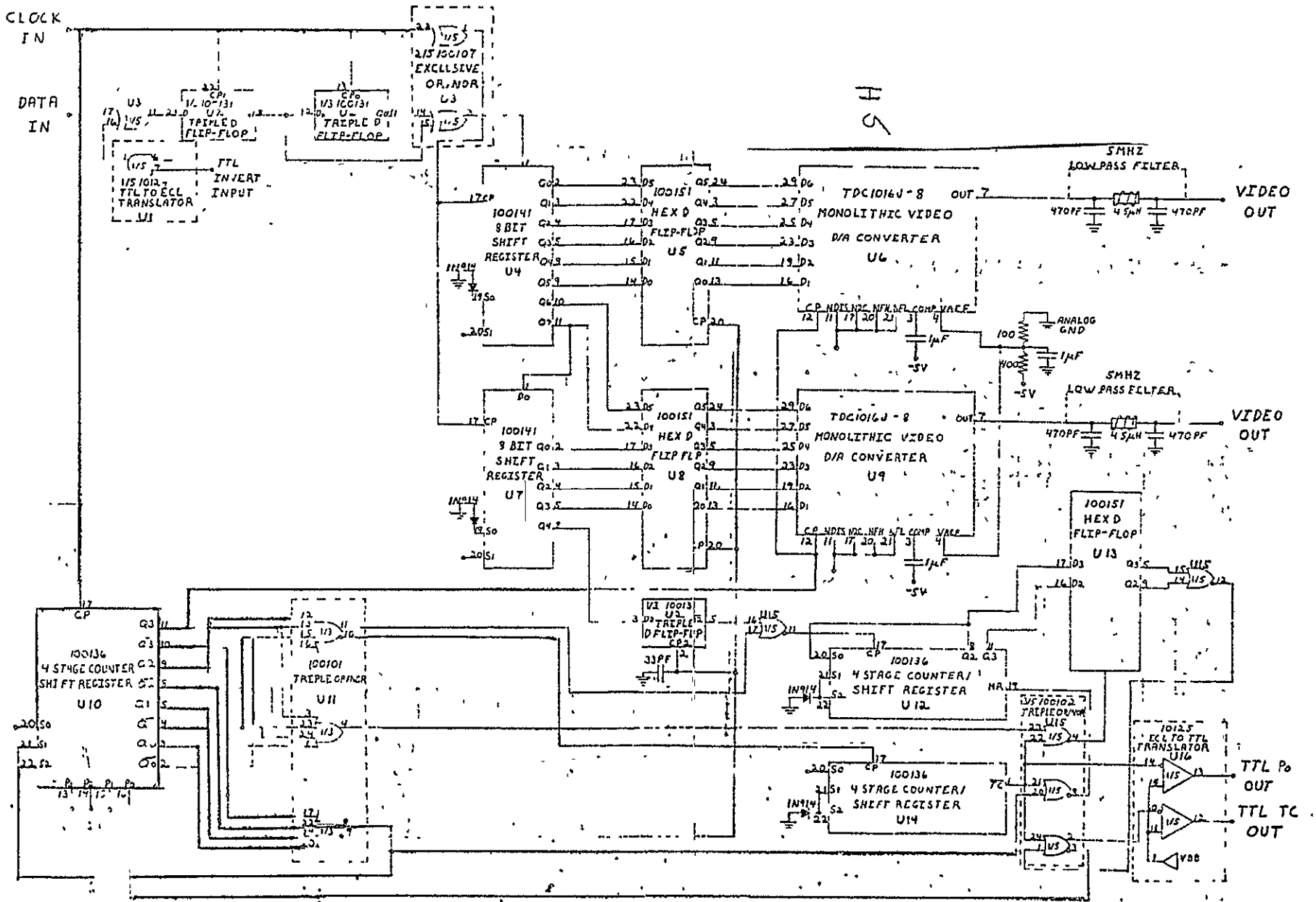


CLOCK RECOVERY SCHEMATIC DRAWING 2



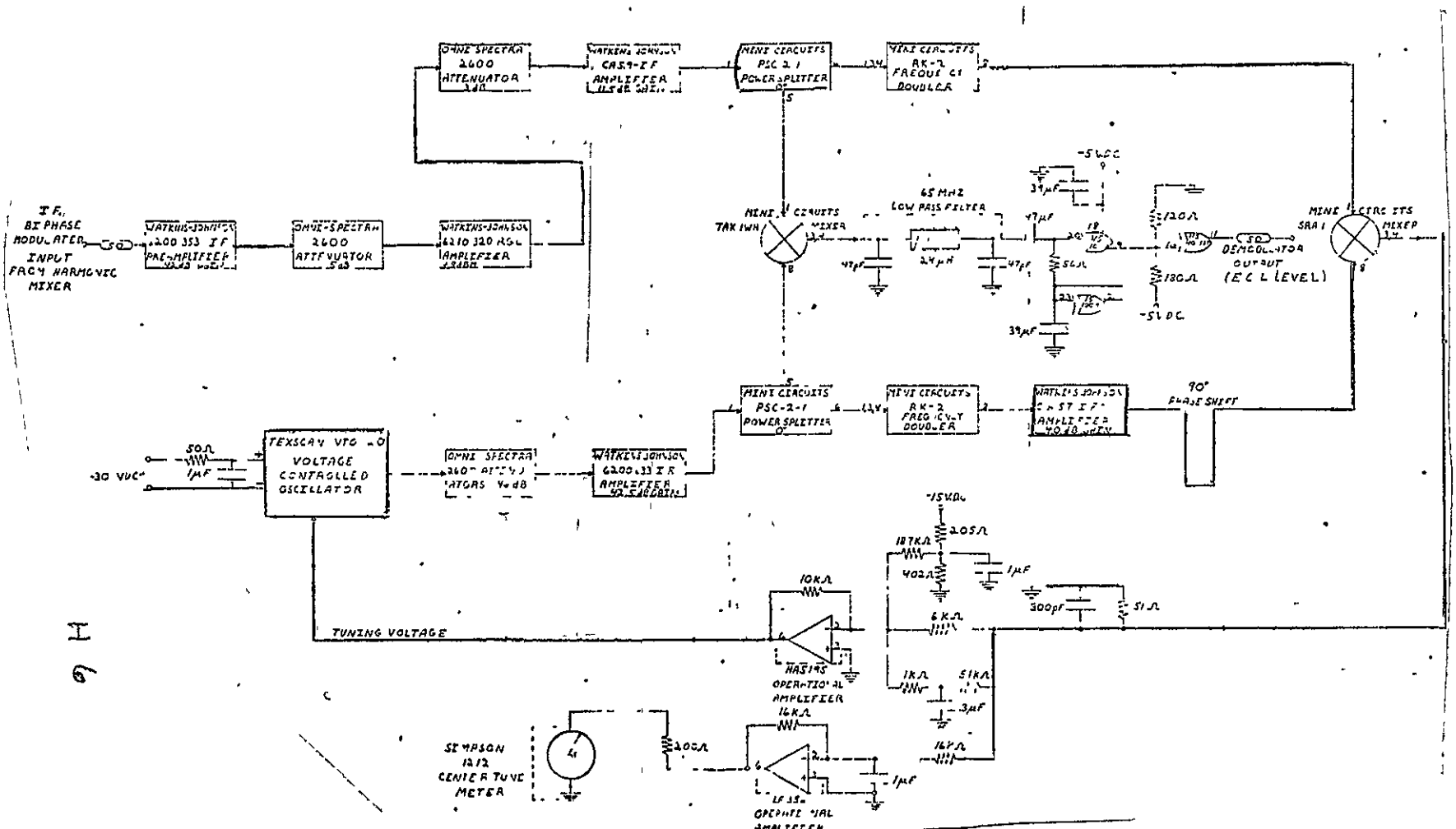
DEMULTIPLEXER AND DUAL VIDEO D/A CONVERTER SCHEMATIC

DRAWING 3

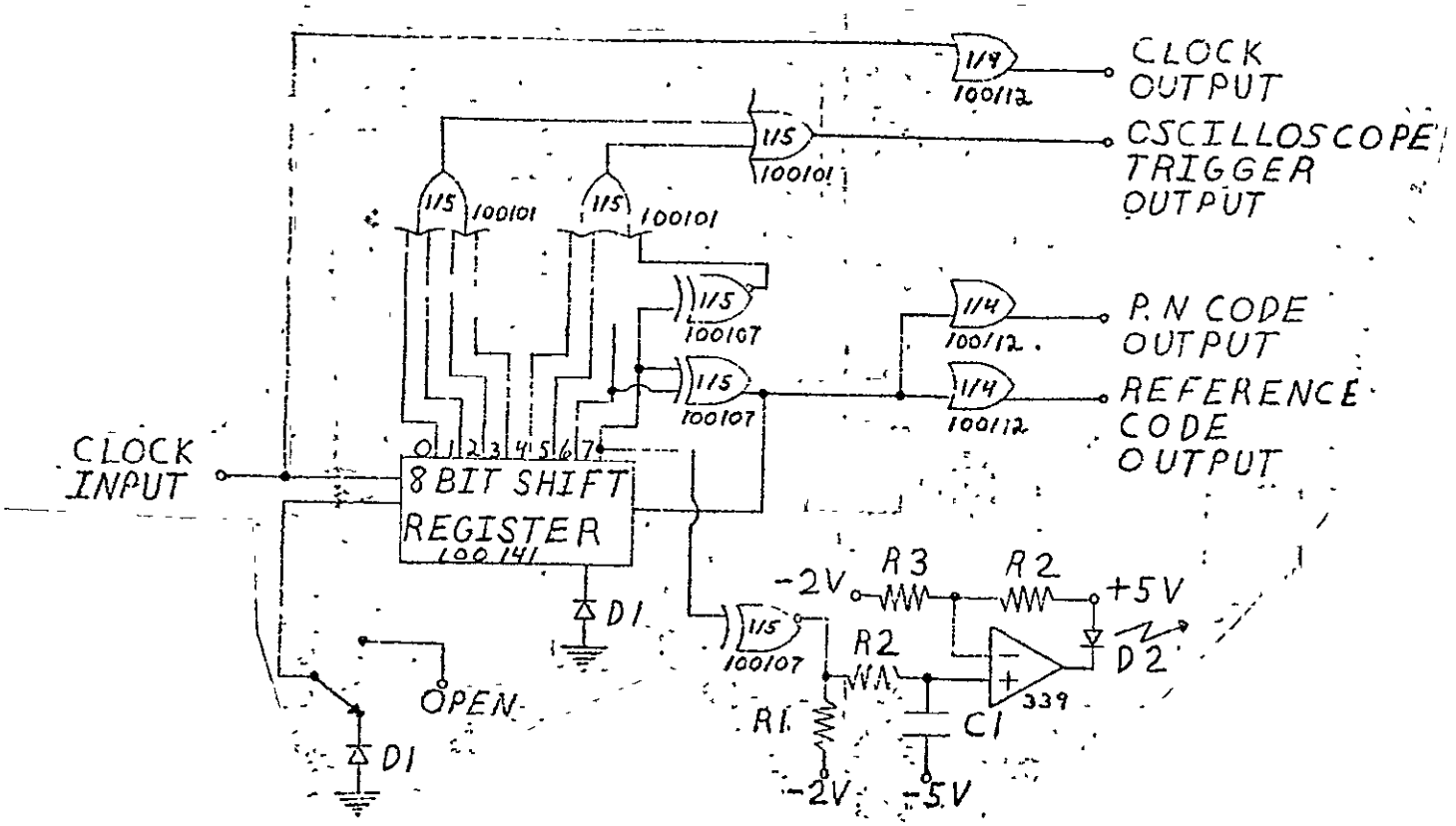


IF AMPLIFIER STRIP / BI PHASE DEMODULATOR SCHEMATIC

DRAWING 4



PSEUDO NOISE CODE GENERATOR
DRAWING 5



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